MULTI-CHANNEL POWER SUPPLY FOR TFT LCD PANELS

BOOST REGULATOR, CHARGE PUMPS, GPM, OP AMP, RESET

FEATURES

- 2.5V to 5.5V Input Voltage Range
- Current Mode Boost Regulator
  - Built-in 18V, 3A, 0.2Ω N-MOSFET
  - 1.2MHz Fixed Switching Frequency
  - Fast Load Transition Response
- Positive Charge Pump Regulator
- Negative Charge Pump Regulator
- High Voltage Switch with Gate Pulse Modulation
  - Adjustable Power On Delay Time
- Operational Amplifier for VCOM Buffer
  - ±200mA Short-Circuit Current
  - 40V/μs Slew Rate
- $\overline{\text{RESET}}$
  - Adjustable Detecting Voltage
  - N-Channel Open-Drain Output
- Soft Start and Power On Sequencing
- Protections
  - Input Under-Voltage Lockout (UVLO)
  - Over-Voltage Protection (OVP)
  - Under Voltage Protection (UVP)
  - Thermal Shutdown (OTP)
- VQFN24 4x4x0.9mm Package Available

APPLICATIONS

- LCD Smart Panel
- LCD Notebook Panel
- LCD Monitor Panel
- LCD TV Panel

GENERAL DESCRIPTION

The AAT1176B device provides a boost regulator, two regulated charge pumps, an operational amplifier, a high voltage switch for gate pulse modulation (GPM), and one open drain reset output, making the device ideal for powering TFT LCD panels.

The current mode boost regulator provides a fast transient response supply voltage for the source driver ICs. It provides an output voltage up to 18V from input voltages ranging from 2.5V to 5.5V. The boost regulator integrates a low R_{DSON} (0.2Ω) N-MOSFET, and operates at a fixed switching frequency of 1.2MHz, thereby minimizing board space while providing good efficiency.

The positive and negative charge pump regulators provide supply voltages for the TFT LCD's gate drivers. Both output voltages can be adjusted with external resistive voltage dividers. For improving TFT LCD image quality, a gate pulse modulation circuit shapes the gate-on signal. The slope of the gate-on voltage and GPM power on delay time can be set by external resistor and capacitor.

The operational amplifier drives the LCD backplane (VCOM). This unity-gain buffer is capable of rail-to-rail input and output, ±200mA output short-circuit current, and a 40V/μs slew rate.

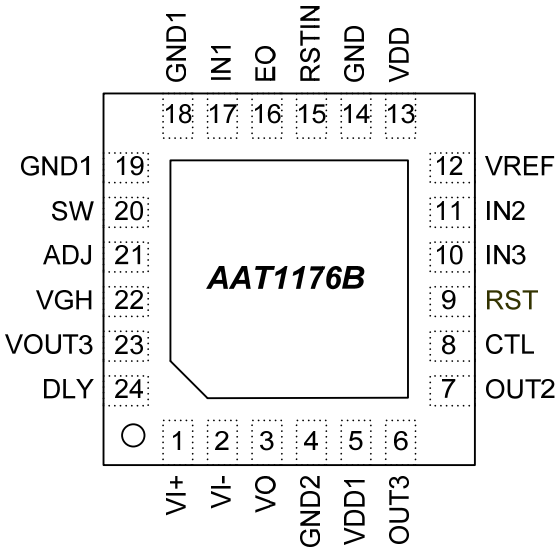
The $\overline{\text{RESET}}$ function is used to monitor the device supply voltage. A reset signal is issued via an open drain NMOS when the supply is below a programmable threshold. The threshold is set by external resistors and the delay time is set by an external capacitor.

The AAT1176B regulators feature soft-start to prevent output overshoots and inrushes. Built-in power on sequencing allows for system stability. This device

includes various protection features such as input under-voltage lockout (UVLO) and over temperature shutdown. Regulator outputs include overload fault protection.

The AAT1176B is available in a small 4x4x0.9mm, ultra-thin, 24 pin VQFN package with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40°C to +85°C ambient temperature range.

PIN CONFIGURATION

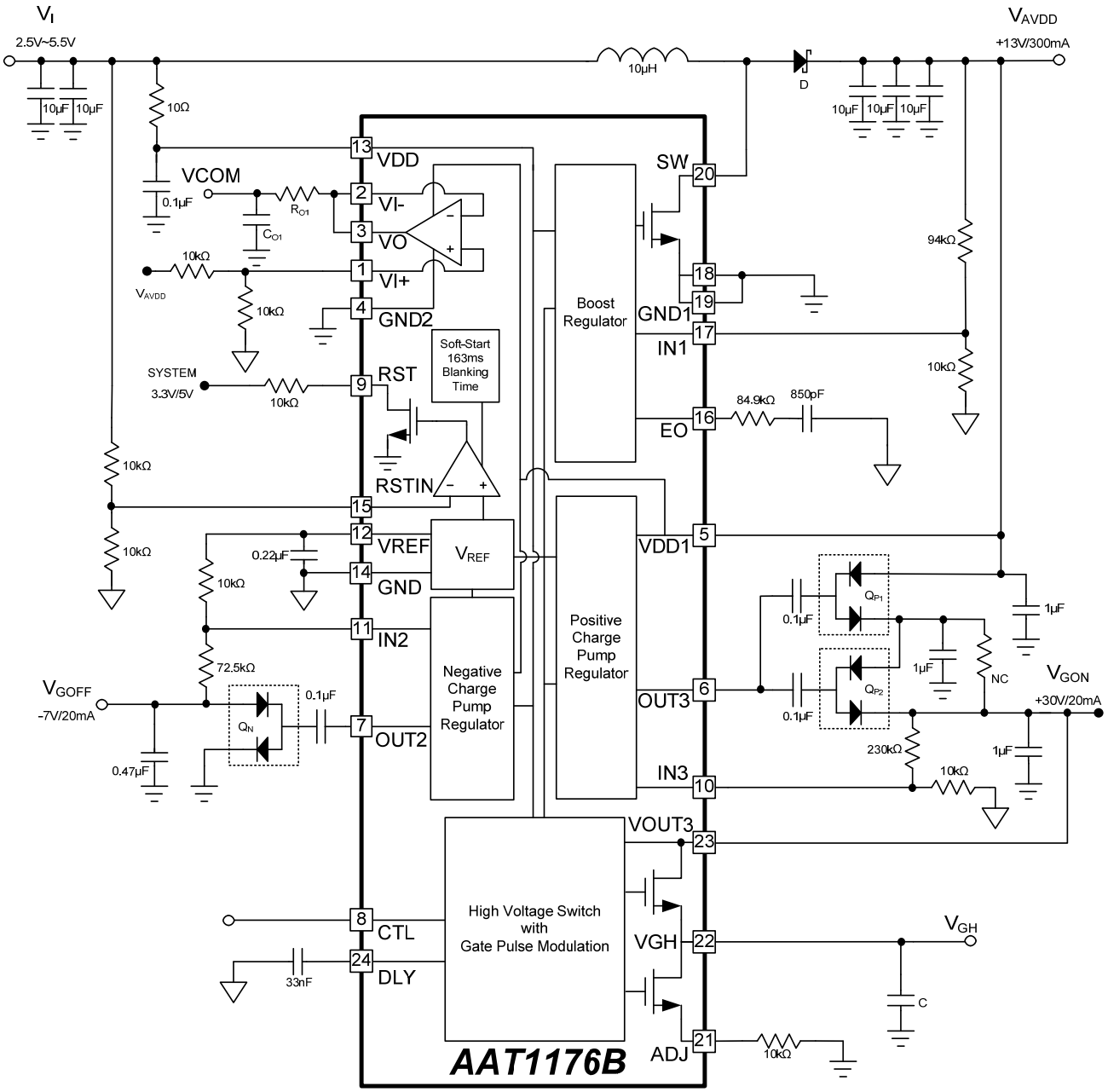


ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1176B	AAT1176B-Q7-T	Q7:VQFN 24-4x4	T: Tape and Reel	–40°C to +85°C	AAT1176B XXXXX XXXX	Device Type Lot no. (6~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VDD, RST to GND	V_{DD}	–0.3 to +7.0	V
VDD1, SW to GND1	V_{H1}	–0.3 to +20	V
VOUT3 to GND1	V_{H2}	–0.3 to +36	V
Input Voltage 1(IN1, IN2, IN3, CTL, RSTIN)	V_{I1}	–0.3 to (V_{DD} +0.3)	V
Input Voltage 2 (VI+, VI–)	V_{I2}	–0.3 to (V_{H1} +0.3)	V
Output Voltage 1 (EO, VREF, DLY)	V_{O1}	–0.3 to (V_{DD} +0.3)	V
Output Voltage 2 (VO, OUT2, OUT3)	V_{O2}	–0.3 to (V_{H1} +0.3)	V
Output Voltage 3 (ADJ, VGH)	V_{O3}	–0.3 to (V_{H2} +0.3)	V
Operating Ambient Temperature Range	T_C	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Range	θ_{JA}	36	°C
Power Dissipation @ T_C = +25°C , T_J = +125°C	P_d	2.78	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at 25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDD Input Voltage Range	V_{DD}		2.5	-	5.5	V
VDD1 Input Voltage Range	V_{DD1}		6	-	18	V
VDD Under Voltage Lockout	V_{UVLO}	Falling	2.05	2.15	2.25	V
		Rising	2.15	2.25	2.35	V
VDD Operating Current	I_{DD}	V_{IN1} = 1.5V, Not Switching	-	0.5	0.95	mA
		V_{IN1} = 1.2V, Switching	-	2.3	5.0	mA
VDD1 Operating Current	V_{DD1}	V_{VI+} = 5V	-	1.2	3.0	mA

Reference Voltage

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Voltage	V_{REF}	I_{VREF} = 100µA	1.238	1.250	1.262	V
Line Regulation		I_{VREF} = 100µA V_{DD} = 2.5V to 5.5V	-	2	5	%/V
Load Regulation		I_{VREF} = 0 to 100µA	-	1	5	%/A

Oscillator (Boost)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillation Frequency	f_{OSC}		1.0	1.2	1.4	MHz
Maximum Duty Cycle	D_{MAX}		86	90	94	%

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C, unless otherwise specified. Typical values are tested at 25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

Soft Start & Fault Detect

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Boost Soft Start Time	t_{SS1}		-	10	-	ms
VGOFF Soft Start Time	t_{SS2}		-	3.4	-	ms
VGON Soft Start Time	t_{SS3}		-	3.4	-	ms
During Fault Protect Trigger Time	t_{FP}		-	55	-	ms
IN1 UVP Trip Level	V_{f1}		0.95	1.00	1.05	V
IN2 UVP Trip Level	V_{f2}		0.40	0.45	0.50	V
IN3 UVP Trip Level	V_{f3}		0.95	1.00	1.05	V
IN1 SCP Trip Level	V_{f4}		-	0.1	-	V

Error Amplifier (Boost)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IN1 Feedback Voltage	V_{IN1}		1.238	1.250	1.262	V
IN1 Input Bias Current	I_{Leak1}	V_{IN1} = 1V to 1.5V	–40	-	+40	nA
IN1 Line Regulation	-	V_{DD} = 2.5V to 5.5V	-	0.05	0.15	%/V
IN1 Load Regulation	-	0< I_{LOAD} < Full	-	1	-	%
Transconductance	g_m	ΔI = 5μA	70	105	240	μS
Voltage Gain	A_V		-	1,400	-	V/V

Switching NMOS (Boost)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SW Current Limit	I_{LIM}		2.5	3.0	-	A
SW NMOS On-Resistance	R_{ON_SW}	I_{SW} = 1.0A	-	0.2	-	Ω
SW Leakage Current	I_{Leak2}	V_{SW} = 15V	-	0.01	20.00	μA

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C, unless otherwise specified. Typical values are tested at 25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

Charge Pump Regulator (gate-on and gate-off)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD1 Input Supply Range	V_H		6	-	18	V
VDD1 Over Voltage Protect	V_{OVP}		-	18	20	V
Charge Pump Frequency	f_{OSCP}		500	600	700	kHz
IN2 Feedback Voltage	V_{H2}		0.235	0.250	0.265	V
IN3 Feedback Voltage	V_{H3}		1.23	1.25	1.27	V
IN2 Input Bias Current	I_{Leak3}	V_{IN2} = –0.25V to 0.25V	–40	-	+40	nA
IN3 Input Bias Current	I_{Leak4}	V_{IN3} = 1V to 1.5V	–40	-	+40	nA
OUT2 Switch On-Resistance	R_{ON_N2}	NMOS	-	3	20	Ω
	R_{ON_P2}	PMOS	-	3	20	Ω
OUT3 Switch On-Resistance	R_{ON_N3}	NMOS	-	3	20	Ω
	R_{ON_P3}	PMOS	-	3	20	Ω

$\overline{\text{RESET}}$

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
RST Output Voltage	V_{RST}	I_{RST} = 1.2mA	-	-	0.2	V
RSTIN Feedback Voltage	V_{INR}		1.23	1.25	1.27	V
RSTIN Hysteresis	V_{RHYS}		-	50	-	mV
RSTIN Input Bias Current	I_{Leak5}		–40	-	+40	nA
RST Blanking Time	t_{BLK}		146	163	180	ms

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at 25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

Operational Amplifier for VCOM Buffer

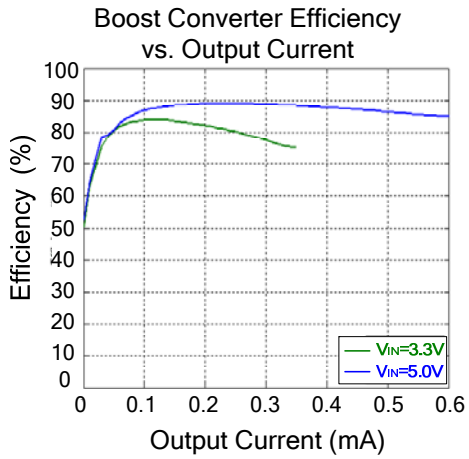
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	V_{VI+} = 5V	-	2	15	mV
Input Bias Current	I_{B5}	V_{VI+} = 5V	–40	-	+40	nA
Output Swing	V_{OH}	I_{VO} = –50mA, V_{VI+} = 5V	-	5.03	5.06	V
		I_{VO} = 5mA, V_{VI+} = 10V	9.85	9.92	-	V
	V_{OL}	I_{VO} = 50mA, V_{VI+} = 5V	4.94	4.97	-	V
		I_{VO} = –5mA, V_{VI+} = 0V	-	0.08	0.15	V
Short Circuit Current	I_{SHORT}	Measure I_{VO}	-	±350	-	mA
Slew Rate	SR	V_{VI+} = 2V to 8V, V_{VI+} = 8V to 2V, 20% to 80%	-	40	-	V/µs
Settling Time	t_S	V_{VI+} = 4.5V to 5.5V, 90%	-	5	-	µs

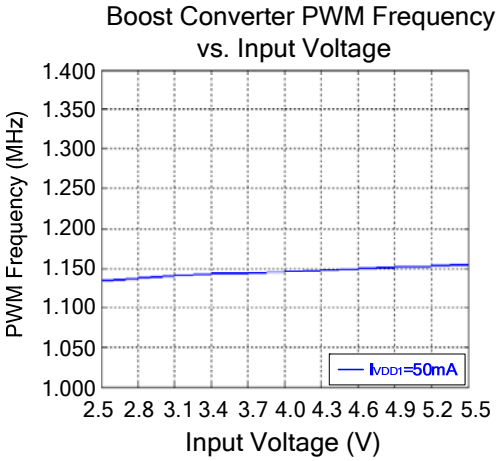
High Voltage Switch with Gate Pulse Modulation

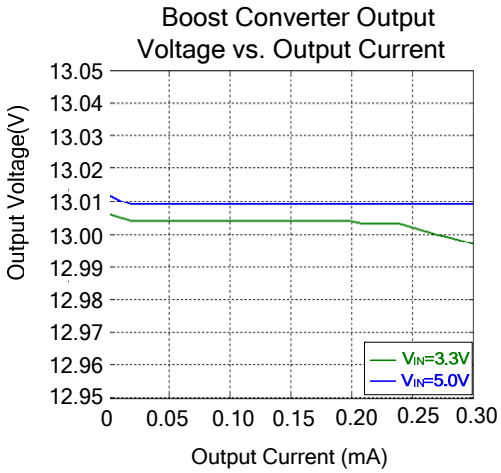
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DLY Source Current	I_{DLY}		4	5	6	µA
DLY Threshold Voltage	V_{DLY}		1.22	1.25	1.28	V
DLY Discharge On-Resistance	R_{DLY}		-	8	-	Ω
CTL Input Low Voltage	V_{IL}		-	-	0.5	V
CTL Input High Voltage	V_{IH}		2	-	-	V
CTL Input Bias Current	I_{B4}	V_{CTL} = 0 to V_{DD}	–40	-	+40	nA
Propagation Delay CTL to VGH	t_{PP}	OUT3 = 25V	-	100	-	ns
VOUT3 to VGH Switch On-Resistance	R_{ON_SC}	V_{DLY} = 1.5V, V_{CTL} = V_{DD}	-	15	30	Ω
ADJ to VGH Switch On-Resistance	R_{ON_DC}	V_{DLY} = 1.5V, V_{CTL} = GND	-	30	60	Ω
VGH to GND1 Switch On-Resistance	R_{ON_CG}	V_{DLY} = 1V	1.5	2.5	3.5	kΩ

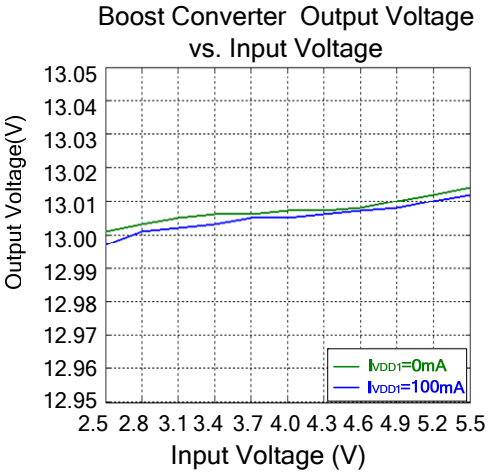
TYPICAL OPERATING CHARACTERISTICS

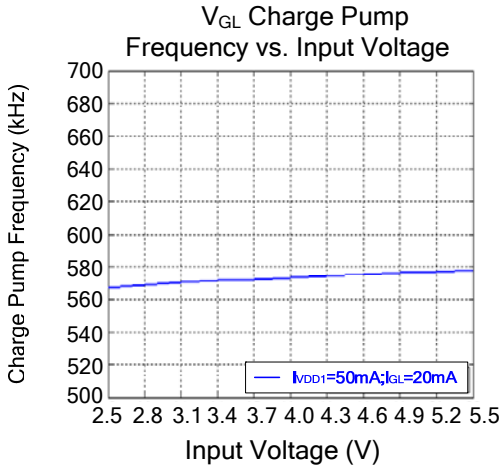
(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

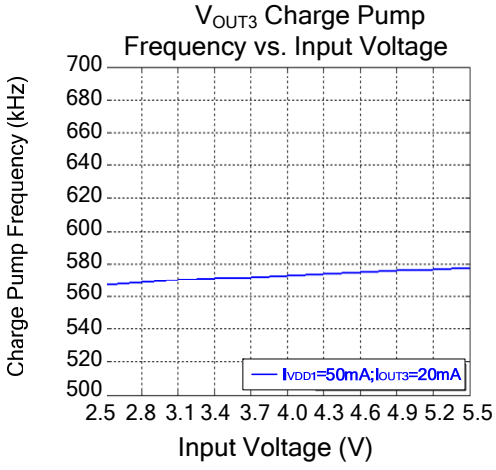








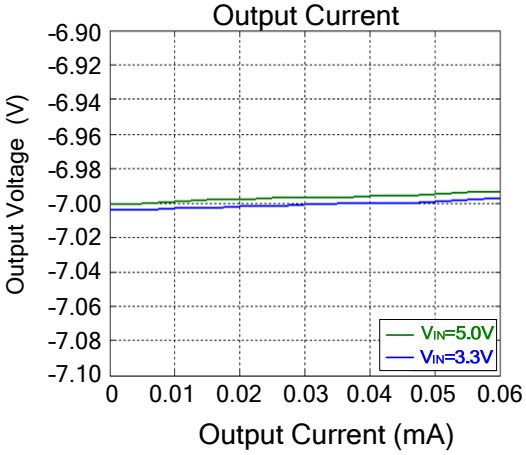




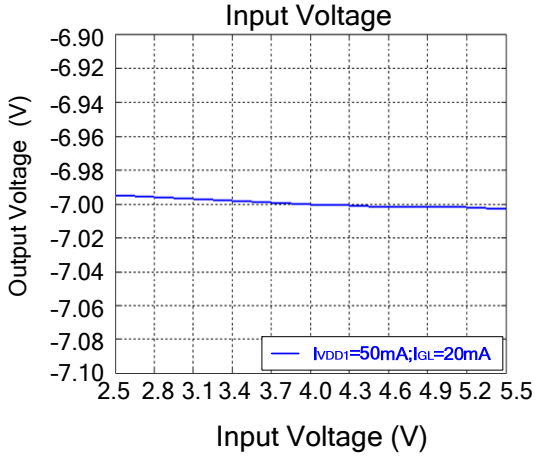
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

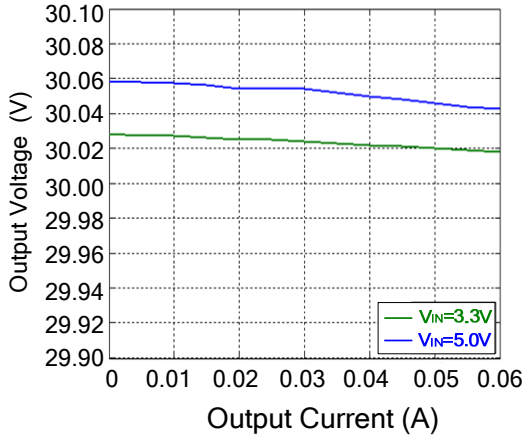
V_{GL} Output Voltage vs. Output Current



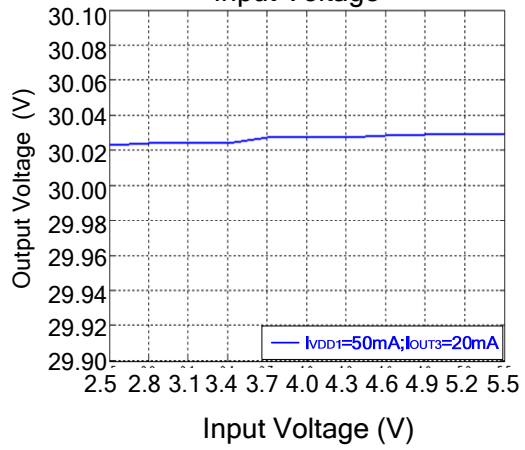
V_{GL} Output Voltage vs. Input Voltage



V_{OUT3} Output Voltage vs. Output Current



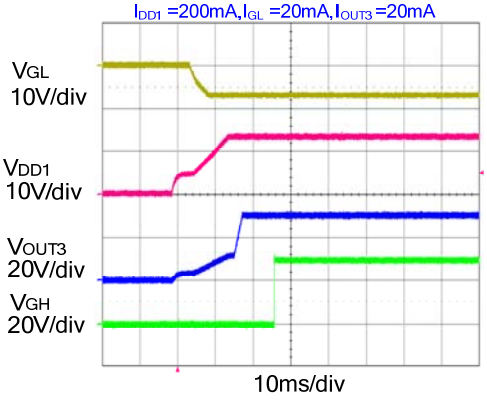
V_{OUT3} Output Voltage vs. Input Voltage



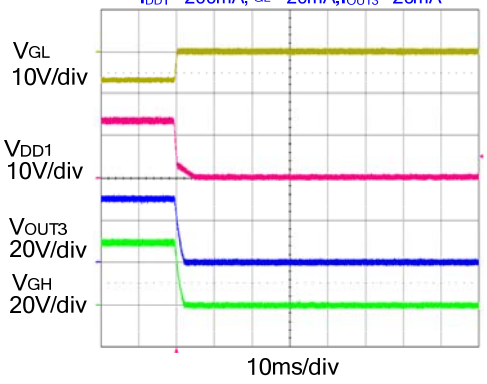
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

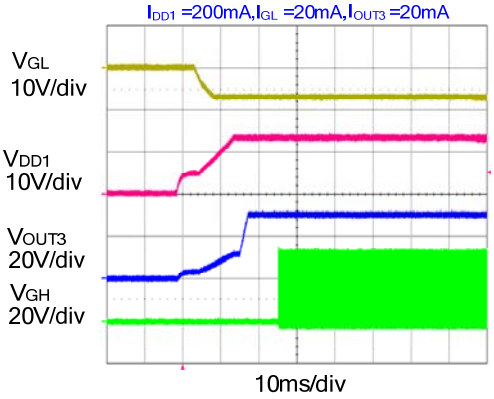
Power On Sequence
C_{TL}=V_{IN}, ADJ=N.C
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



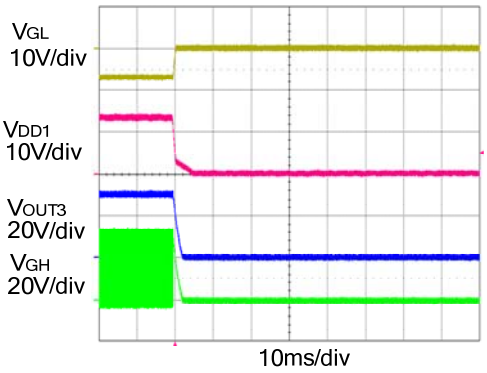
Power Off Sequence
C_{TL}=V_{IN}, ADJ=N.C
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



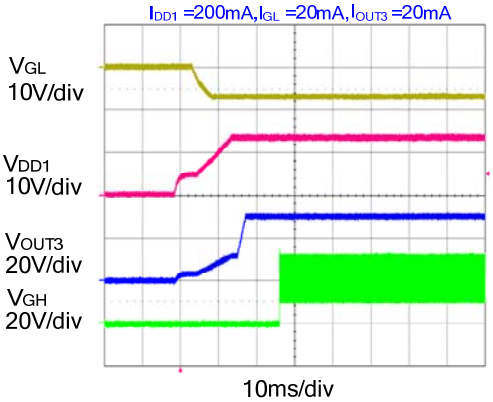
Power On Sequence
C_{TL}=Signal, ADJ=GND
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



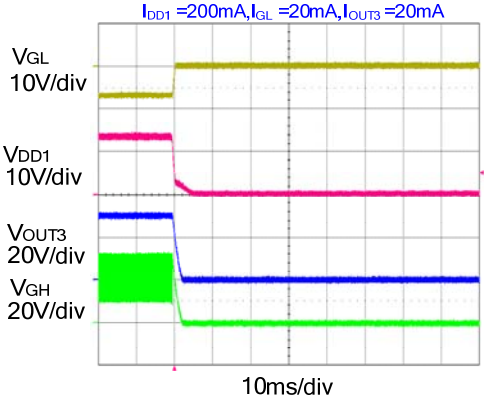
Power Off Sequence
C_{TL}=Signal, ADJ=GND
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



Power On Sequence
C_{TL}=Signal, ADJ=VDD1
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



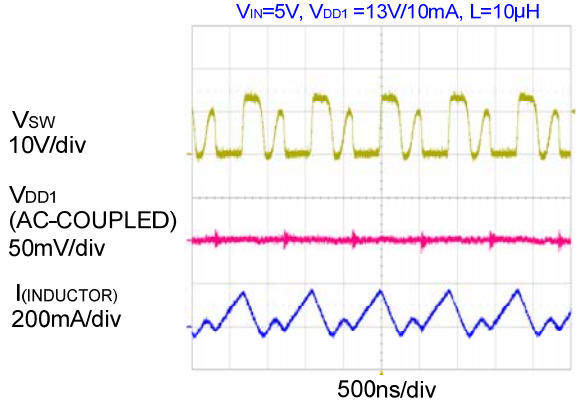
Power On Sequence
C_{TL}=Signal, ADJ=VDD1
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



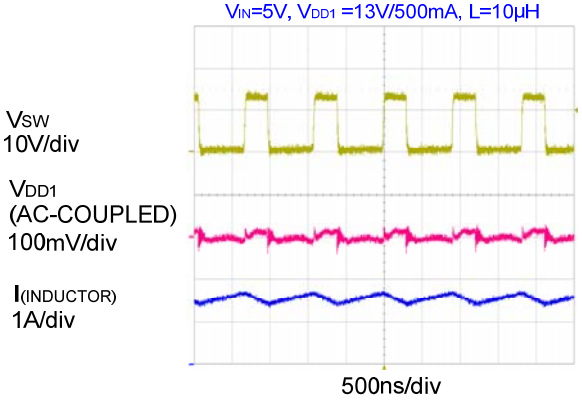
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

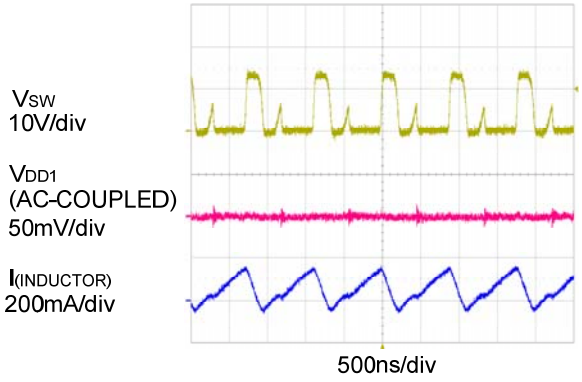
Boost Converter PWM
Discontinuous Mode: Light Load
V_{IN}=5V, V_{DD1} =13V/10mA, L=10µH



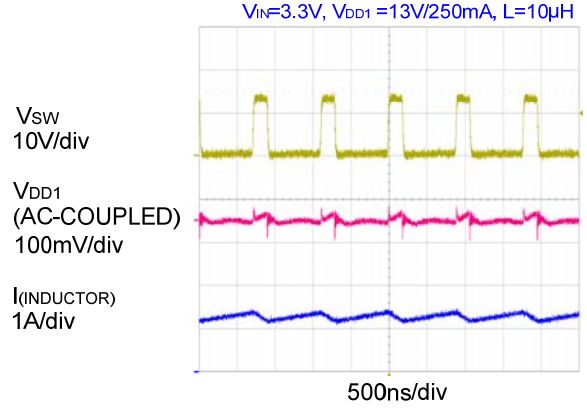
Boost Converter PWM
Discontinuous Mode: Heavy Load
V_{IN}=5V, V_{DD1} =13V/500mA, L=10µH



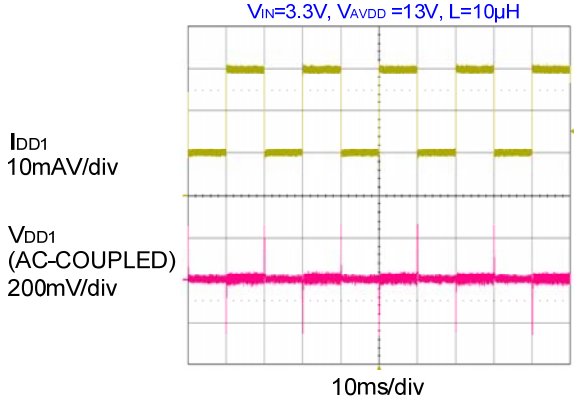
Boost Converter PWM
Discontinuous Mode: Light Load
V_{IN}=3.3V, V_{DD1} =13V/5mA, L=10µH



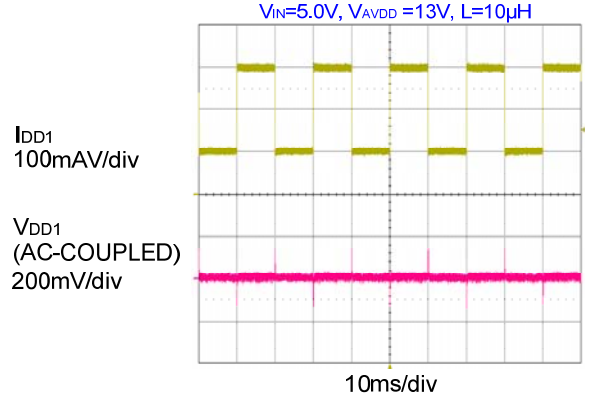
Boost Converter PWM
Discontinuous Mode: Heavy Load
V_{IN}=3.3V, V_{DD1} =13V/250mA, L=10µH



Boost Converter Load Transient
Response
V_{IN}=3.3V, V_{AVDD} =13V, L=10µH



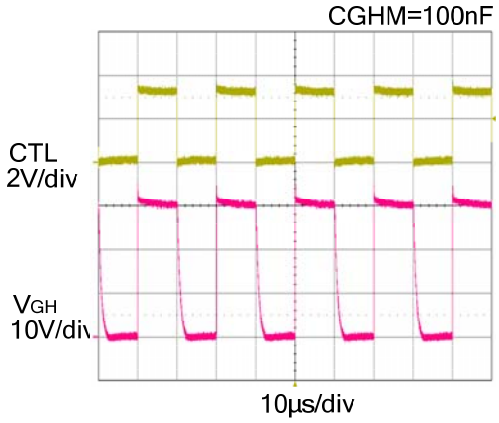
Boost Converter Load Transient
Response
V_{IN}=5.0V, V_{AVDD} =13V, L=10µH



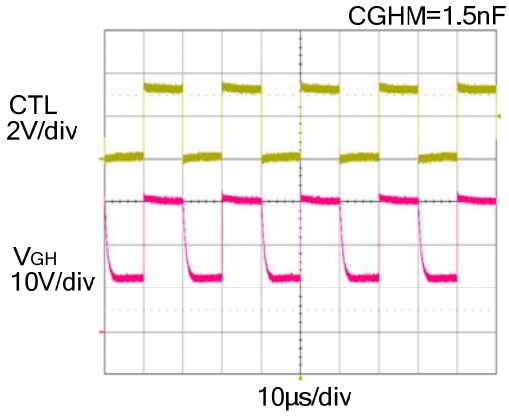
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

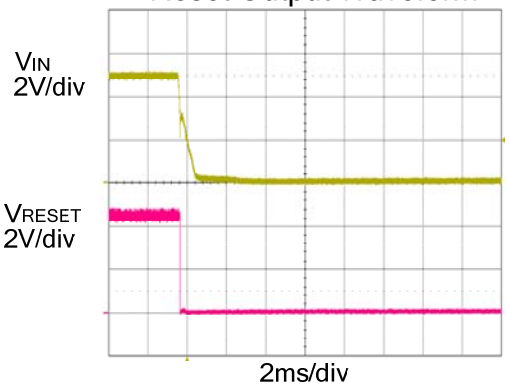
High Voltage Switch Control Waveform



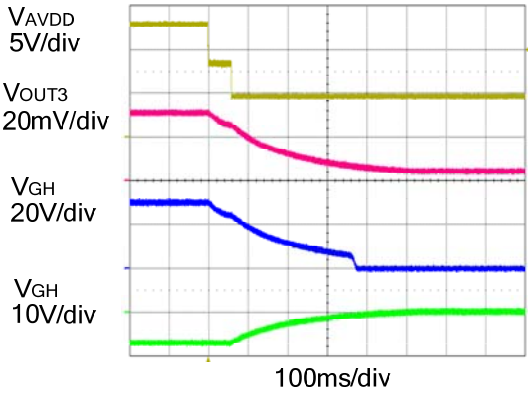
High Voltage Switch Control Waveform



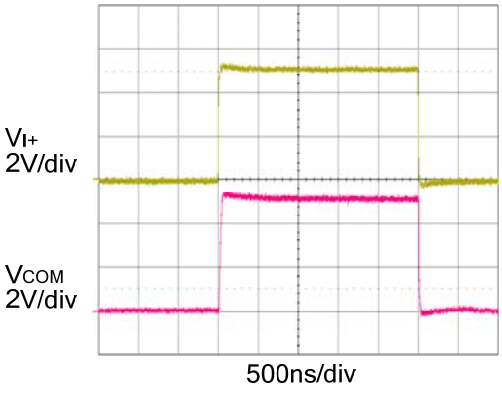
Reset Output Waveform



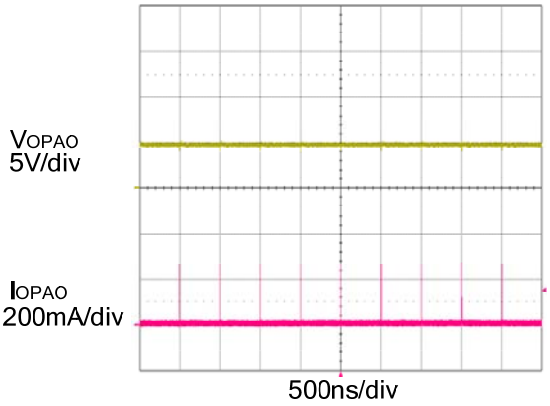
Fault Protection Waveform



V_{COM} Buffer Large Signal Waveform



V_{COM} Buffer Load Transient Response



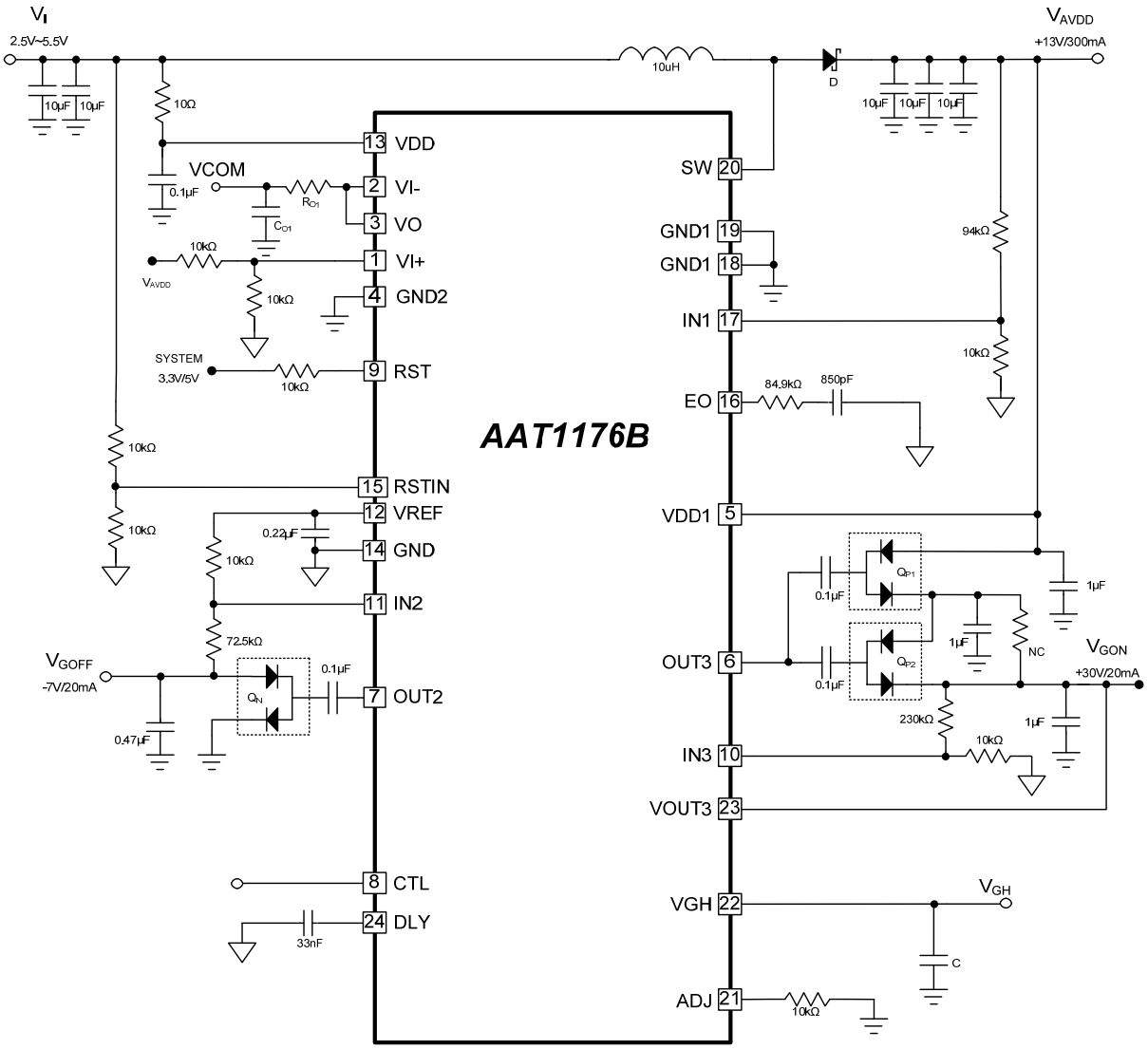
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	VI+	I	Operational Amplifier Non-Inverting Input
2	VI-	I	Operational Amplifier Inverting Input
3	VO	O	Operational Amplifier Output
4	GND2	-	Operational Amplifier Ground. Typically Referenced to Power Ground
5	VDD1	I	Operational Amplifier and Charge Pumps Power Supply. Typically Supplied by Connecting the Output of the Boost to VDD1
6	OUT3	O	Positive Charge Pump Output Drive
7	OUT2	O	Negative Charge Pump Output Drive
8	CTL	I	High Voltage Switch Control. When CTL is Logic High, the Switch Between VGH and VOUT3 is Turned on While the Switch Between ADJ and VGH is Turned off. When CTL is Logic Low, the Switch Between VGH and VOUT3 is Turned off While the Switch Between ADJ and VGH is Turned on
9	RST	O	Reset Signal Open Drain Output. Pulled High Via a 10kΩ Resistor to the System Supply
10	IN3	I	Positive Charge Pump Feedback. Reference for Regulating the Output of the Positive Charge Pump
11	IN2	I	Negative Charge Pump Feedback. Reference for Regulating the Output of the Negative Charge Pump
12	VREF	O	Internal Reference Voltage Output. Bypass to Analog Ground with a 0.22μF Capacitor
13	VDD	I	Boost Power Supply. Power for the Internal Reference Voltage and Low Voltage Circuitry. Bypass, as Close as Possible from the VDD Pin to Analog Ground, with A 0.1μF Capacitor
14	GND	-	Analog Ground
15	RSTIN	I	Reset Comparator Input. Use to Monitor the Input Supply Voltage for the IC Device Via an External Resistive Divider
16	EO	O	Boost Error Amplifier Compensation Output
17	IN1	I	Boost Feedback. Reference Input for the Boost Regulator
18	GND1	-	SW MOS Ground or Power Ground
19	GND1	-	SW MOS Ground or Power Ground
20	SW	-	Boost Switching Output. Switch Node for the Boost Regulator. Point of Connection Between the External Boost Inductor and Anode of the Free Wheeling Diode

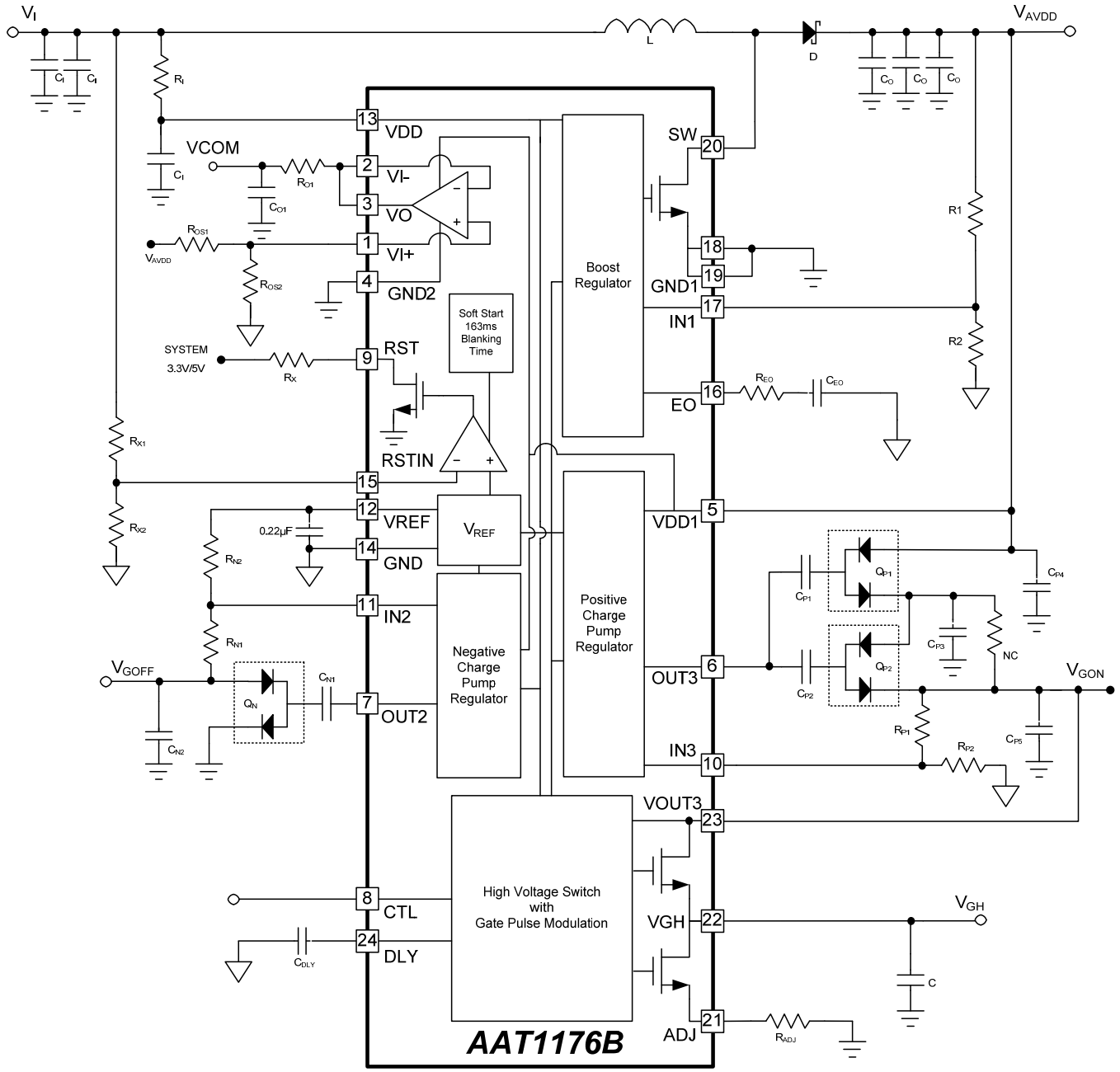
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
21	ADJ	O	Gate High Voltage Switching Output Falling Time Setting
22	VGH	O	Gate High Voltage Switching Output for TFT LCD Gate-On Driver
23	VOUT3	-	Gate High Voltage Switching Input. Supplied by the Positive Charge Pump Regulated Output
24	DLY	I	Gate High Voltage Switching Turn on Delay Adjust. Connect a Capacitor from DLY to Ground to Set the Delay Time

TYPICAL APPLICATION CIRCUIT



FUNCTIONAL BLOCK DIAGRAM



THEORY OF OPERATION

The AAT1176B offers a complete solution for powering TFT LCD panels. The device integrates a boost regulator for the source driver, a positive charge pump regulator for the gate-on driver, a negative charge pump regulator for gate-off, a high voltage switch with gate pulse modulation for flick compensation, an operational amplifier for supplying the LCD backplane VCOM, and various system protection schemes such as soft start, power up sequencing, fault protection, thermal shutdown, and supervisory reset.

Boost Regulator

The boost regulator uses a peak current mode control scheme that provides fast output recovery during transients, and also simple compensation. The 1.2MHz fixed high switching frequency allows for smaller output inductor and ceramic capacitors. Together with an integrated low R_{DSON} (typical 0.2Ω) NMOS, built-in soft start, the AAT1176B saves board space for the system designer. The boost regulator operates from an input voltage range of 2.5V to 5.5V, and delivers an output ranging from V_I to a voltage that reaches the maximum capable duty cycle. The duty cycle (D) is calculated by

$$D = \frac{V_O - V_I}{V_O} \quad \text{or} \quad \frac{V_O}{V_I} = \frac{1}{1-D}, \quad (V_O = V_{AVDD})$$

where V_O (V_{AVDD}) is the output of the boost regulator. Typical maximum duty cycle is approximately 90%.

At the heart of the current mode topology are two feedback loops. See the AAT1176B Boost Regulator Functional Block Diagram Figure 1. One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal power switch. The second loop monitors the boost output via a resistive divider to the IN1 and compares the IN1 voltage to an internal reference voltage of 1.25V using a transconductance error amp. Regulation is achieved by modulating the internal power switch ON time. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles above 50%. During each rising edge of the internal clock pulse, the power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

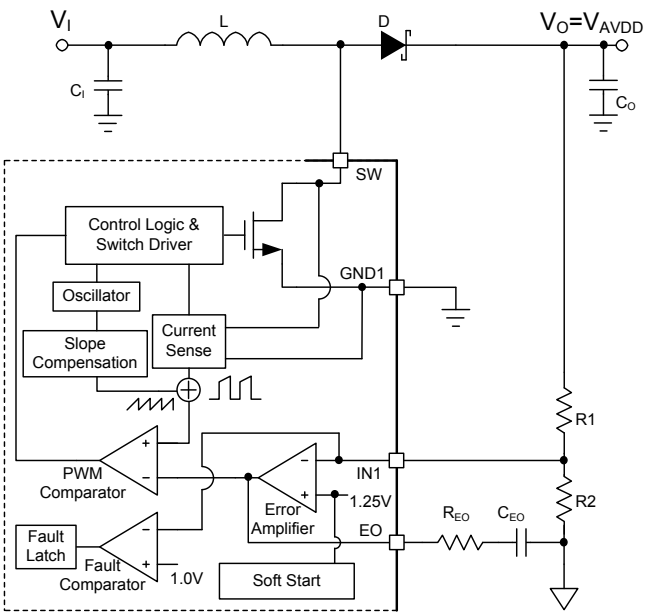


Figure 1. AAT1176B Boost Regulator Functional Block Diagram

The boost regulator includes fault protection. When the voltage at IN1 is below the fault protection threshold of 1V for more than 55ms, the boost will be disabled. In addition, all other regulators will also shut down.

Positive Charge Pump Regulator

The positive regulated charge pump provides a step-up supply for the TFT LCD panel gate-on driver. The achievable output voltage is determined by the number of charge pump stages. For example, for achieving a maximum capable of approximately 3x the input voltage will require a two stage charge pump as shown in Figure 2. However, the actual regulated voltage is set by an external resistive divider from V_{GON} to GND with center tap connected to IN3.

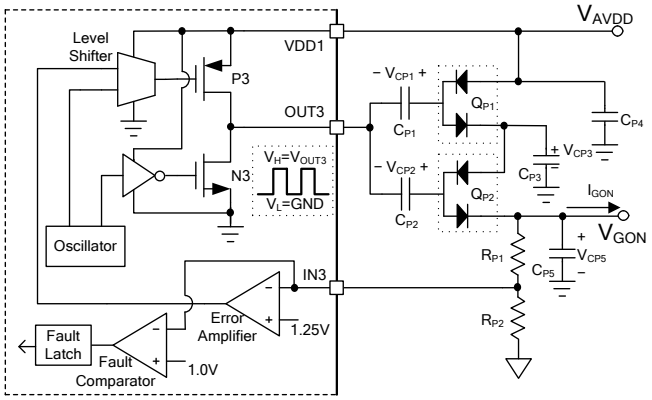


Figure 2. Positive Charge Pump Regulator Functional Block Diagram

The positive charge pump consists of a high side PMOS (P3) and low side NMOS (N3) both controlled by an internal oscillator switching frequency of 640kHz. Initially, when the oscillator output is logic Low, P3 is turned off while N3 is turned on, pulling the charge pump drive output low (V_{OUT3} = GND), recharging the flying capacitors C_{P1} and C_{P2} by the input supply V_{AVDD} and V_{CP3}. Thus

$V_{CP1} = V_{AVDD} - V_D$

$V_{CP2} = V_{CP3} - V_D$ where $V_{CP3} = V_{AVDD} - 2V_D + V_{OUT3}$

V_D : the voltage drop across the diode

When the oscillator output is logic High, P3 is turned on while N3 is turned off, pulling the charge pump drive output to a high potential V_{OUT3}, and level shifting the flying capacitors. If the output capacitors are at a lower potential, by more than a diode drop than the level shifted flying capacitors, charge will flow from the flying capacitors to the output capacitors to replenish the output charge. Thus,

$V_{CP3} = V_{AVDD} - 2V_D + V_{OUT3}$

$V_{CP5} = V_{GON} = V_{CP2} - V_D + V_{OUT3}$

$V_{GON} = V_{AVDD} - 4V_D + 2V_{OUT3}$

When V_{OUT3} is approximately equal to V_{AVDD}, the voltage at V_{GON} is approximately 3x the input voltage V_{AVDD}. This is the maximum achievable output voltage for the two stage charge pump.

When the high side PMOS is on while the low side NMOS is off, the charge pump drive output V_{OUT3} will be pulled high to a voltage magnitude that is dependent on the output power requirement. For example, as the output load increases, the feedback voltage at IN3 will initially fall, increasing the error amplifier output drive strength and also the charge pump drive output voltage to a higher level. This increase in voltage of the charge pump drive output high level provides more charge to the flying capacitors and to the output for regulation. Likewise, when the output power demand drops, the charge pump drive output voltage during the high level will decrease.

The positive charge pump regulator includes fault protection. When the voltage at IN3 is below the fault protection threshold of 1V for more than 55ms, the charge pump will be disabled. In addition, all other regulators will also shut down.

Charge Pump Flying Capacitors

Use a 0.1µF ~ 0.47µF for the flying capacitors (C_{P1}, C_{P2}) and make sure that the voltage rating (V_{CP}) of these capacitors is adequate per the number of stages. The voltage rating of the capacitor must satisfy

$V_{CP} > n \times V_{AVDD}$

where V_{AVDD} is the input supply to the charge pumps, and n is the number of stages per charge pump. Note that the positive charge pump uses 2 stages, i.e. n = 2.

Charge Pump Output Capacitors

The output capacitor (C_{PO}) for the charge pump is selected to satisfy the output ripple requirement. Use ceramics for low ESR to minimize the ripple. The capacitance value can be found by

$$C_{PO} > \frac{I_{GON}}{2 \times f_{OSC} \times \Delta V_{RIPPLE}}$$

where ΔV_{RIPPLE} is the output ripple specification, f_{OSC} is 640kHz.

Positive Charge Pump Output Setting

The positive charge pump output voltage (V_{GON}) is set with external resistor ladder from its output to ground with the center tap connected to IN3 pin, as shown in Figure 2, Use the following equation,

$$R_{P1} = R_{P2} \times \left(\frac{V_{GON}}{V_{IN3}} - 1\right) \quad \text{where} \quad V_{IN3} = 1.25V, R_{P2} = 10k\Omega$$

Negative Charge Pump Regulator

The negative regulated charge pump generates a negative supply for the TFT LCD panel gate-off driver. The maximum output voltage capability is determined by the number of charge pump stage, but the actual regulated output voltage is set via a resistive divider to VREF, with the center tap connected to IN2. Typical application uses a single stage, as shown in Figure 3.

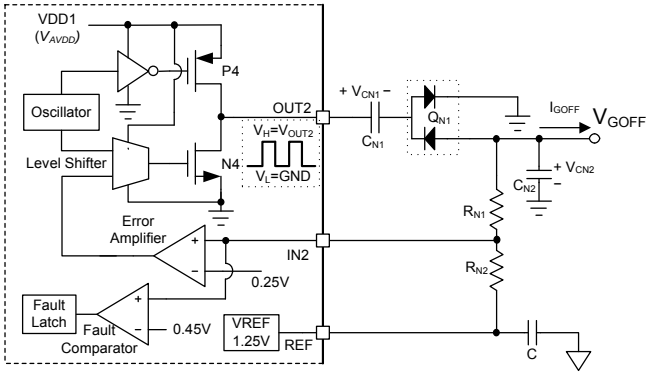


Figure 3. Negative Charge Pump Regulator Functional Block Diagram

The regulation scheme of the negative charge pump also consist of a high side and low side switch for charging, level shifting the flying capacitor, and drawing charge from the output. When the high side PMOS (P4) is turned on and the low side NMOS (N4) is off, the flying capacitor C_{N1} will charge as the upper diode will turn on and create a path to ground, and $V_{CN1} + V_D = V_{OUT2}$. When the drive output OUT2 pulls low to near ground, the flying capacitor C_{N1} is level shifted in the negative direction, and the node connecting between C_{N1} and Q_{N1} becomes ($-V_{CN1}$). Thus, charge will flow from the output C_{N2} to C_{N1}, and the output can be expressed as

$(-V_{CN1}) = V_{CN2} - V_D \rightarrow V_{CN2} = (-V_{CN1}) + V_D$

$V_{CN2} = V_{GOFF} = (-V_{OUT2}) + 2V_D$ where ($V_{CN1} = V_{OUT2} - V_D$)

The voltage magnitude of V_{OUT2} when pulled high will vary, as this voltage is dependent on the output power requirement. The maximum capable output voltage at V_{OUT2} when the P4 is fully turned ON is V_{AVDD}. Thus, the maximum capable output of this single stage charge pump is

$V_{GOFF} = V_{CN2} = (-V_{AVDD}) + 2V_D$

The negative charge pump regulator also includes fault protection. When the voltage at IN2 rises above 0.45V for more than 55ms, this charge pump is disabled. In addition, all other regulators will also shut down.

Charge Pump Flying Capacitors

Use a 0.1µF ~ 0.47µF for the flying capacitor (C_{N1}) and make sure that the voltage rating (V_{CN}) of these capacitors is adequate per the number of stages. The voltage rating of the capacitor must satisfy

$V_{CN} > n \times V_{AVDD}$

where V_{AVDD} is the internal supply to the charge pumps, and n is the number of stages per charge pump. Note that the negative charge pump uses 1 stage, i.e. n = 1.

Charge Pump Output Capacitors

The output capacitor (C_{NO}) for the charge pump is selected to satisfy the output ripple requirement. Use ceramics for low ESR to minimize the ripple. The capacitance value can be found by

$$C_{NO} > \frac{I_{GOFF}}{2 \times f_{OSC} \times \Delta V_{RIPPLE}}$$

where ΔV_{RIPPLE} is the output ripple specification, f_{OSC} is 640kHz.

Negative Charge Pump Output Setting

The output voltage (V_{GOFF}) of the negative charge pump is set with an external resistor ladder from its output to VREF, with the center tap connected to IN2, as shown in Figure 3. Use the following equation to calculate the required output voltage.

$$R_{N1} = R_{N2} \times \frac{\left(V_{GOFF} - V_{IN2}\right)}{\left(V_{IN2} - V_{REF}\right)}$$

where V_{IN2} is 0.250V and V_{REF} is 1.250V, R_{N2}=10kΩ.

High Voltage Switch with Gate Pulse Modulation (GPM)

An internal high voltage switch controller is included for gate pulse modulation which provides gate shaping to improve image quality in TFT LCD applications. The circuitry consist of two high voltage PMOS, one between VOUT3 and VGH, and another between VGH and ADJ. See Figure 4 for the Gate Pulse Modulation Functional Block Diagram. When the switch controller is enabled, logic level on the CTL input will determine which PMOS switch is ON or OFF. If CTL is logic High, P5 turns on and P6 turns off, VGH connects to VOUT3. If CTL is logic Low, P5 turns off and P6 turns on, VGH connects to ADJ, and the V_{GH} output is discharged via the resistor connected at ADJ to ground. Note that the resistor (R_{ADJ}) value can be adjusted to different discharge time or high to low transient slope rate.

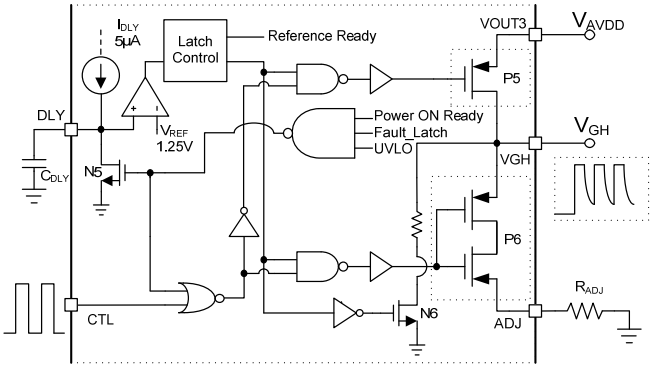


Figure 4. Gate Pulse Modulation Functional Block Diagram

The GPM must be enabled for the CTL input to control the PMOS switches. When the device supply voltage has exceeded the UVLO threshold, soft start has completed for V_{GOFF}, V_{AVDD}, V_{GON} or device is power on ready, and no fault condition is present, an internal 5µA current source will begin to charge the external capacitor connected to the DLY. While this capacitor is charging, the VGH will be pulled to ground via an internal resistor and NMOS (N6). When the voltage at DLY exceeds V_{REF} (1.25V), the NMOS switch (N6) will be turned off, the GPM will be enabled, and CTL will control the PMOS switches as described above.

During operation, if the input supply falls below the UVLO threshold, the GPM will be immediately disabled. Instantly, the high side PMOS P5 will turn on, the low side PMOS P6 will turn off simultaneously, and CTL input will have no control over the PMOS switches.

C_{DLY} Time Delay Setting

After device power up and soft start for the three regulators have completed, a 5µA current source will begin charging the external capacitor (C_{DLY}) connected at the DLY to ground. When the voltage at the DLY exceeds V_{REF} (1.25V), the switch control block will be enabled. The capacitor (C_{DLY}) to set the enable delay time (t_D) is chosen using the following formula

$$C_{DLY} = t_D \times \frac{I_{DLY}}{V_{REF}} \quad \text{where } I_{DLY} = 5\mu A, V_{REF} = 1.25V$$

Operational Amplifier for VCOM Buffer

The operational amplifier drives the LCD backplane (VCOM) or the gamma-correction divider string. The Op Amp is capable of rail-to-rail input and output, ±200mA output short-circuit current, and a 40V/µs slew rate. In typical application, the inverting input is shorted to the output for a unity-gain (voltage follower) configuration.

In the unity-gain configuration, the capacitive load adds a pole to the loop gain that impacts the stability of the system and leads to output peaking, ringing and oscillation. A higher pole frequency results in greater stability. In fact, if the pole frequency is lower than or close to the unity gain frequency, the pole can have a significant negative impact on phase and gain margins. Therefore, the stability decreases when the capacitive load increases.

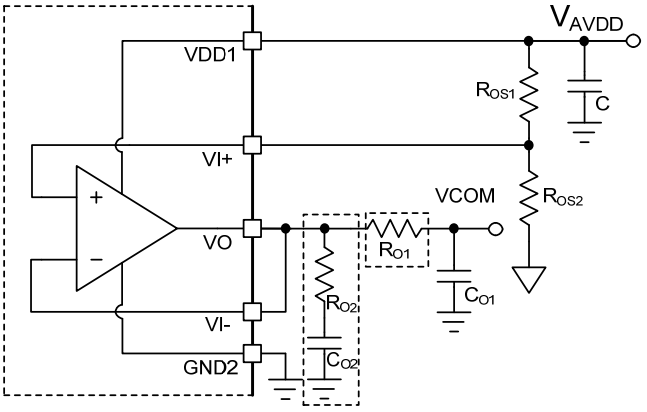


Figure 5. Operational Amplifier Functional Block Diagram

One method of improving capacitive load drive is to insert a 2Ω to 20Ω resistor (R_{O1}) in series with the output, as shown in Figure 5. This reduces ringing with large capacitive loads while maintaining DC accuracy.

Another method for improving transient response is to add a snubber circuit at the output. A snubber circuit consists of a resistor (R_{O2}) in series with a capacitor (C_{O2}), which improves output settling time and reduces peaking. The advantage of this topology is that it draws no DC current nor does it reduce the gain.

VCOM Buffer Output Setting

The VCOM Buffer output voltage (VCOM) is set with external resistor ladder from its output to ground with the center tap connected to VI+ pin, as shown in Figure 5, Use the following equation,

$$R_{OS1} = R_{OS2} \times \left(\frac{V_{AVDD}}{V_{COM}} - 1\right)$$

Where V_{AVDD} is the output voltage of boost regulator, R_{OS2} = 10kΩ.

$\overline{\text{RESET}}$

This device has an internal reset circuit to monitor the voltage at RSTIN pin. In typical application, the input supply (V_I) is monitored by connecting a resistive divider from the input to ground, with center tap connected to RSTIN. When the RSTIN voltage is lower than the threshold voltage of V_{REF} (1.25V), RST output will be pulled low. RST is an open-drain output that needs a pull-up resistor (10kΩ) to a system supply. During initial device power up, when VDD rises above its UVLO threshold, a 163ms blanking time is initiated in which any voltage drop below 1.25V is ignored for the duration.

As shown in Figure 6 for $\overline{\text{RESET}}$ Functional Block Diagram, use the following equation to calculate the required resisters of R_{X1} and R_{X2}.

$$R_{X1} = R_{X2} \times \left(\frac{V_I}{V_{REF}} - 1\right)$$

where V_{REF} is 1.250V and R_{X2}=10kΩ.

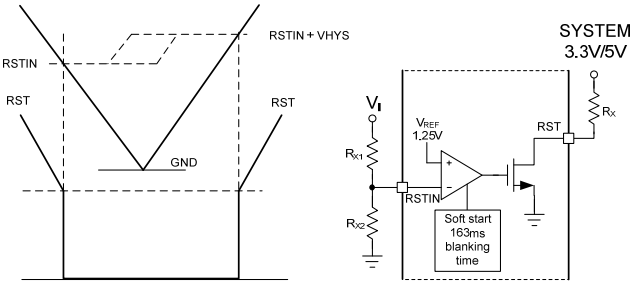


Figure 6. $\overline{\text{RESET}}$ Functional Block Diagram

Reference Voltage (V_{REF})

The reference output voltage is 1.250V. The reference voltage can be used to regulate the negative charge pump and source at least 100µA. In order to have a stable reference voltage, connect a 0.22µF ceramic bypass capacitor between VREF and GND.

Under Voltage Lockout (UVLO)

For systematic startup, AAT1176B employs a UVLO threshold of 2.25V. Thus, the input supply must exceed the UVLO threshold for the regulators to begin startup. Likewise, the device shuts down all functions when the input voltage is lower than UVLO falling threshold of 2.15V. A 50mV hysteresis is added to prevent device chattering when the input supply is noisy or unstable during power up or power down.

Soft Start and Power-On Sequence

Soft start for each regulator is controlled by an internal 7-bit DAC to minimize inrush current and output overshoot. For the boost regulator and positive charge pump, the DAC controller ramps up the reference voltage in 128 steps. Similarly, the DAC controller steps down the reference voltage to 0.25V for the negative regulated charge pump. Upon device startup, a fixed-frequency clock drives the DAC controller to generate the soft start time. The boost regulator soft start time is typically 10ms; the two regulated charge pumps for gate-off and gate-on has a soft start time of typically 3.4ms.

When input VDD is applied or initially turned ON, as VDD exceeds approximately 1.5V, the V_{REF} (1.25V) internal reference starts to ramp up and charge its external 0.22µF capacitor. When VDD exceeds the UVLO threshold of 2.25V, the device enables the three regulators. The power on sequence of the three regulators is $V_{GOFF} \rightarrow V_{AVDD} \rightarrow V_{GON}$, which was shown in Figure 7.

The startup delay of high voltage switch control block is determined by an external capacitor connected between DLY and GND. When the input voltage has reached the UVLO rising threshold, soft start for each regulator has been completed, and no fault is detected, a 5µA constant current starts to charge the capacitor. The high voltage switch control block is activated after the capacitor voltage exceeds 1.25V.

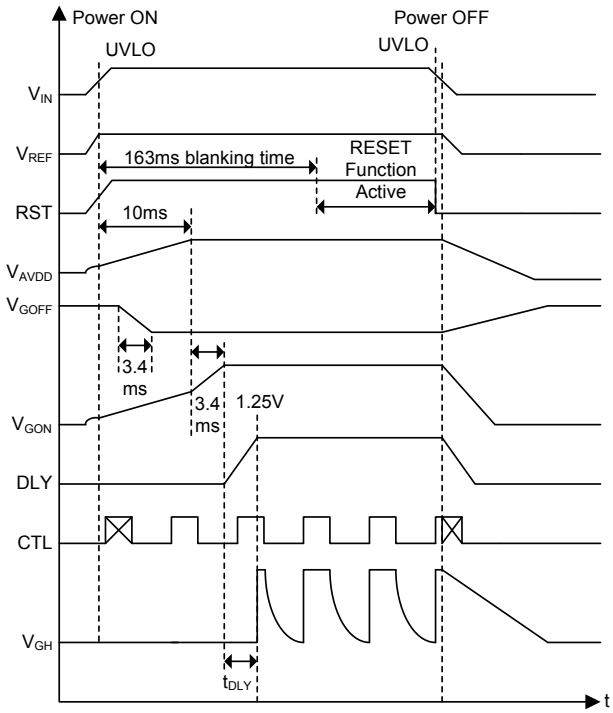


Figure 7. AAT1176B Power On / Off Sequence

Fault Protection

If any one of the three regulators exceeds its Fault Protection Voltage threshold, an internal fault timer of 55ms is activated. Once activated, if the fault condition surpasses the 55ms, the device will shutdown all three regulators but will keep the internal reference at 1.25V. Note that fault protection is only active after all soft start events have completed.

Thermal Shutdown

The device enters into fault protection shutdown when the junction temperature reaches approximately 160°C. As described earlier, when in fault protection shutdown, all three regulators are disabled except for the internal reference. To restart the device, the junction temperature must reduce by approximately 15°C, and VDD power must be recycled below the UVLO falling threshold.

APPLICATION NOTE

Boost Regulator

The AAT1176B integrates a current-mode, PWM Boost and NMOS switch. Figure A1 shows the AAT1176B Boost Regulator Functional Block Diagram.

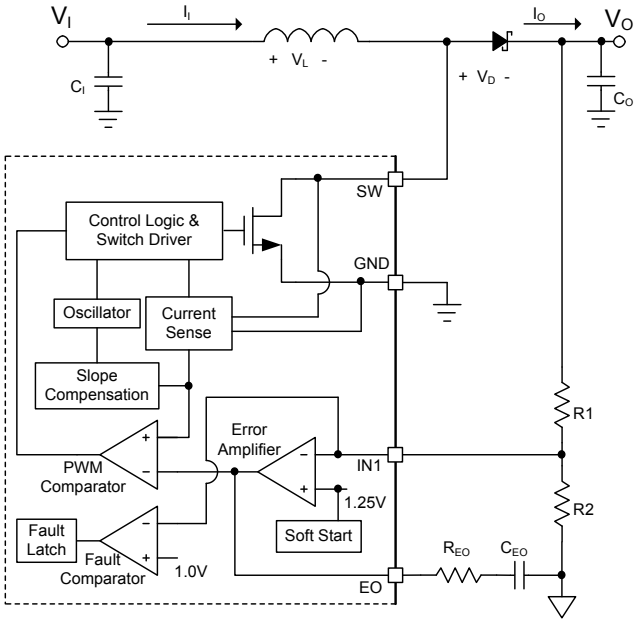


Figure A1. Boost Regulator Functional Block Diagram

The boost regulator steps the input voltage up to higher output voltage. The basic configuration of a boost regulator can be seen in Figure A2.

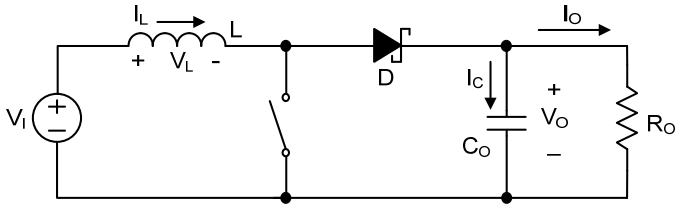
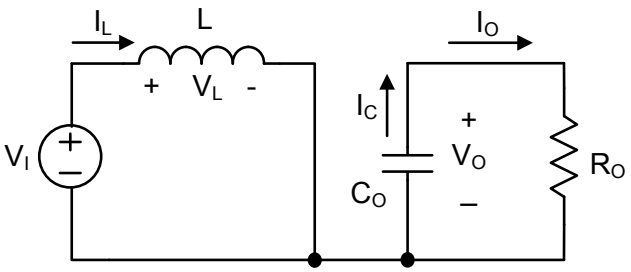


Figure A2. Basic Boost Regulator Topology

The basic boost regulator operates in two time periods. The first time duration (DT_S) occurs when the switch is on, and the diode is reversed biased. This results in a positive voltage $V_L=V_I$ across the inductor. This voltage causes a linear increase in the inductor current I_L. During this "ON" period, energy is stored in the inductor and the load current is supplied by C_O.



Switch Off For The Time Duration DT_S

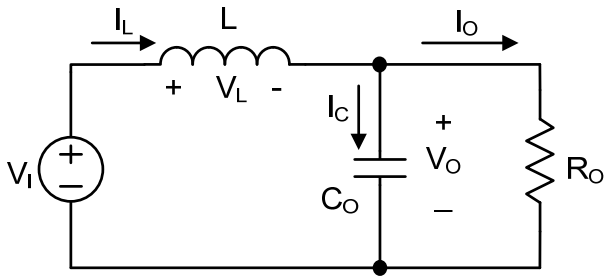


Figure A3. Switch Off For The Time Duration $(1\text{-}D)T_S$

The next time duration is the "OFF" period of the power switch. When the switch is turned off, the diode is forward biased, and the energy stored in the inductor is transferred to the load and output capacitor. The voltage across the inductor reverses its polarity and is clamped by the diode, because of the inductive energy storage, I_L continues to flow. The current now flows through the diode, and $V_L= –(V_O–V_I)$ for a time duration $(1\text{-}D)T_S$ until the switch is turned on again.

Equating the integral of the inductor voltage over one time period to zero yields

$$\int_0^{T_S} V_L(t)dt = \int_0^{DT_S} V_L(t)dt + \int_{DT_S}^{T_S} V_L(t)dt,$$

($D = \frac{t_{ON}}{T_S}$ where T_S is the period of switching)

$$V_I \times DT_S – (V_O – V_I) \times (1–D)T_S = 0$$

$$V_I = (1–D)V_O, \quad \frac{V_O}{V_I} = \frac{1}{1-D}$$

Component Selection for Boost Regulator

Inductor Selection (L)

The value of the inductor is calculated based on the input V_I and output voltage V_O, switching frequency f_{OSC}, and the nominal output load current I_O. However, when selecting the optimal inductance, both the regulator's performance and the inductor size or cost must be considered. According to the operating relationship between inductor voltage and inductor current shown in Figure A4, the Inductor ripple current (ΔI) can be calculated by the following equation.

$$iL(t) = iL(0) + \frac{1}{L}\int V_L(t)dt, \quad \left(T_S = \frac{1}{f_{OSC}}, \quad \frac{V_O}{V_I} = \frac{1}{1-D}\right)$$

$$\Delta I = \frac{1}{L} V_I \times DT_S = -\frac{1}{L}(V_O - V_I) \times (1-D)T_S$$

$$\Delta I = \frac{1}{L} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I)$$

And obtain Inductance L

$$L = \frac{1}{\Delta I} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I),$$

$$\left(\eta = \frac{V_O \times I_O}{V_I \times I_I}, \quad L_{IR} = \frac{\Delta I}{I_I} = \frac{\eta \times V_I}{V_O \times I_O} \times \Delta I\right)$$

$$L = \frac{\eta}{L_{IR}} \times \frac{1}{f_{OSC}} \times \left(\frac{V_I^2 \times (V_O - V_I)}{V_O^2 \times I_O}\right)$$

Where L_{IR} is the ratio of the ripple current (ΔI) to input current (I_I) at the full load current, and η is efficiency.

Although using a small inductance can decrease component size or cost and increase the regulator's response time, inductor ripple current increases which results in high output ripple and in lower efficiency due to increase conduction losses. Using a large inductance can lower ripple current to mitigate conduction losses and minimize output ripple, but too large of an inductance leads to slow response time and lower efficiency if the losses from the higher DCR outweigh the losses eliminated from lower ripple current. The inductor ripple current is usually adjusted by the system designer based on application for the desired cost and performance.

After selecting the inductance value, the inductor's saturation current rating should be chosen to exceed the inductor ripple current for the lowest input voltage V_{I_MIN} in the application.

$$I_{L\_AVE(MAX)} = \frac{V_O \times I_O}{V_{I\_MIN} \times \eta} \quad \left(\text{where } \eta = \frac{V_O \times I_O}{V_I \times I_I}\right)$$

And Inductor peak current I_{L_PEAK}

$$I_{L\_PEAK} = I_{L\_AVE(MAX)} + \frac{1}{2}\Delta I$$

$$I_{L\_PEAK} = \frac{V_O \times I_O}{V_{I\_MIN} \times \eta} + \frac{1}{2L} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I)$$

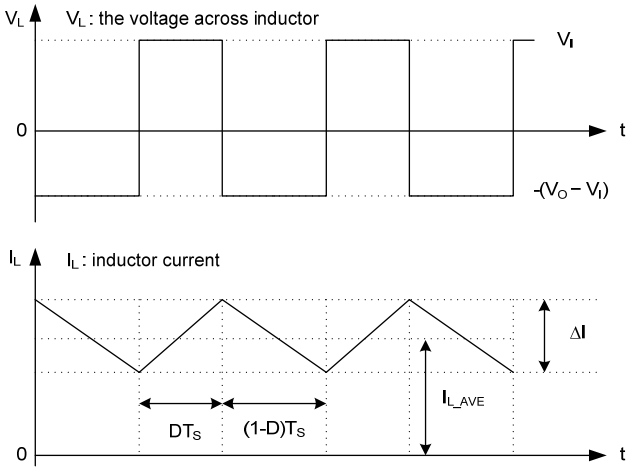


Figure A4. Inductor Voltage vs. Inductor Current (CCM)

For boost regulator, L_{IR} is usually chosen to be 0.3 to 0.5. However, if the inductor used in the TFT LCD application has significant wire resistance, higher L_{IR} (above 0.5) can be used to lower the inductance value and therefore lower the total DCR.

Output Capacitor Selection (C_O)

For switching regulators, output capacitance is chosen based on the desired output ripple and/or output voltage deviation based on a given load change.

The output voltage ripple consists of both the inductor ripple current flowing through the capacitor ESR (equivalent series resistance), and the transfer of charge to and from the output capacitor. Since in TFT LCD display applications, ceramic capacitors are used at the output, the ripple due to the IR effect can be neglected since ceramics capacitors have extremely low ESR. Thus, the ripple due to the charge and discharge of the output capacitor will be dominant. Based on a desired ripple, the minimum output capacitance can be calculated by. (Please refer to the Figure A5)

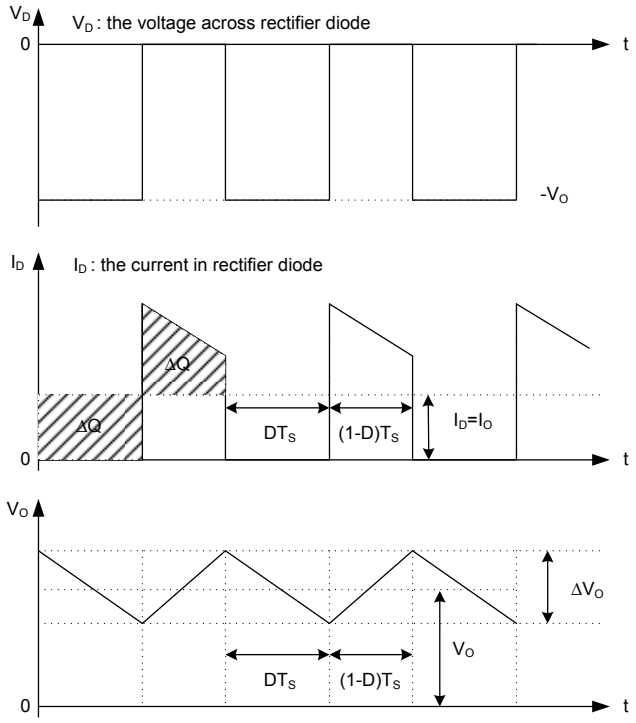


Figure A5.

$$\Delta V_O = \frac{\Delta Q}{C_O} = \frac{I_O \times DT_S}{C_O} \left(Q = CV, T_S = \frac{1}{f_{OSC}}, \frac{V_O}{V_I} = \frac{1}{1-D} \right)$$

$$\Delta V_O = \frac{I_O}{C_O} \times \frac{1}{f_{OSC}} \times \frac{(V_O - V_I)}{V_O}$$

$$C_O = \frac{I_O}{\Delta V_O} \times \frac{1}{f_{OSC}} \times \frac{(V_O - V_I)}{V_O}$$

where ΔV_O is the output ripple voltage specification.

Note that ceramic capacitors are often used for their size advantage and environmentally-friendly nature. To achieve the required ripple or output capacitance value, multiple ceramic capacitors are often connected in parallel.

Input Capacitors Selection (C_I)

Input capacitors are usually a combination of bulk capacitor and high frequency ceramic. The bulk capacitor serves as the power source during the soft start process, supplies switching current, minimizes input ripple, and keeps the DC input voltage stable. The bulk capacitor is usually chosen to support the input RMS current, and can also be ceramic type. Often, extra bulk capacitance is added during bench evaluation to alleviate the parasitic inductance introduced from the power supply cable.

The high frequency ceramic capacitor filters the high frequency noise to the device. Usually, a 0.1µF to 1µF ceramic capacitor is used. A RC low-pass filter is often added to decrease interference from noise.

Diode Selection (D)

The diode voltage rating must be greater than the output voltage V_O and the current rating must exceed the inductor peak current I_{L_PEAK}. Using a diode with low forward voltage drop and fast recovery time to minimize the conduction loss and switching loss, and then help increase efficiency, such as a Schottky rectifier is recommended.

Output Voltage Selection (V_O)

The output voltage is set using a resistive voltage divider from the output to FB1, referenced to analog ground as shown in Figure A1. Use the following equation to set the boost voltage, or V_O,

$$R_1 = R_2 \times (\frac{V_O}{V_{FB1}} - 1)$$

where V_{FB1} is 1.250V and R_2=10kΩ.

Crossover Frequency Selection

The crossover frequency, or the regulator bandwidth, is usually selected to satisfy the output step load requirement. However, due to the inherent nature of the CCM boost, a right-half-plane-zero (RHPZ) will limit the selection of the crossover frequency (f_C) due to its phase lag. A good design rule is to select the crossover frequency to be about 20% of the RHPZ frequency. The RHPZ frequency is given by

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad \text{where} \quad R_O = \frac{V_O}{I_O}$$

$$f_C = 0.2 \times f_{RHPZ}$$

Compensation Selection (R_C & C_C)

To stabilize the boost regulator's loop, a RC series network is added from the COMP output pin to analog ground. See Figure A1. R_C is chosen to set the amplifier gain for a targeted crossover frequency. Setting the total loop gain to unity gain at the desire crossover frequency, we can calculate R_C by approximately

$$R_C = 0.3 \times \frac{V_O}{V_{FB1}} \times \frac{V_O}{V_I} \times \frac{\pi \times f_C \times C_O}{g_m \times g_{CS}}$$

Where g_m=105μS is the feedback error amplifier transconductance, g_{CS}=4S is the current sense transconductance, the crossover frequency of the regulator f_C=20%×f_{RHPZ}, and V_{FB1} is the feedback reference voltage of 1.24V. In typical application, RC value ranges from 10kΩ to 100kΩ.

Once R_C is selected, C_C is adjusted to place a zero for neutralizing the output pole caused by the output capacitance C_O and load R_O. Use the following equation to calculate C_C,

$$C_C = \frac{C_O \times R_O}{50 \times R_C}$$

In typical application, C_C value ranges from 680pF to 2.2nF.

Buck Regulator

The AAT1176B integrated a current-mode, PWM Buck Regulator. Figure B1 shows the AAT1176B Buck Regulator Functional Block Diagram.

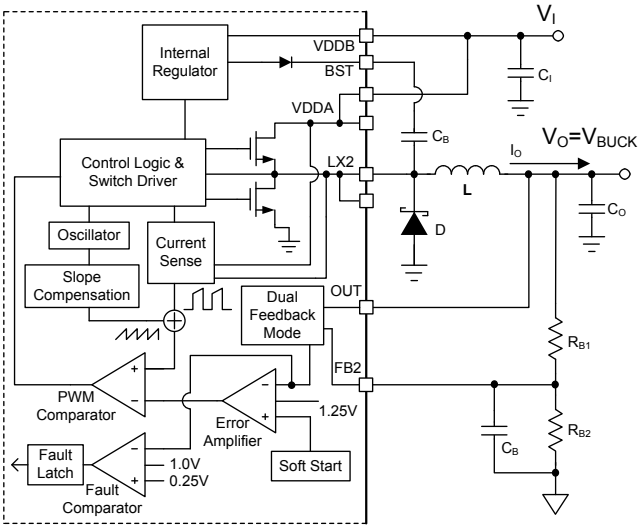


Figure B1. Buck Regulator Functional Block Diagram

The Buck Regulator is the most elementary forward–mode regulator. Its basic schematic can be seen in Figure B2.

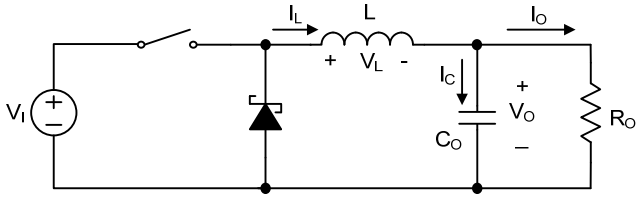
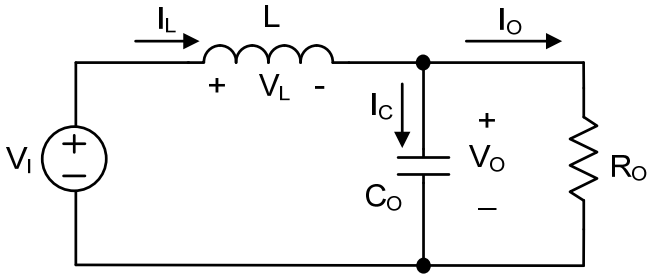


Figure B2. Basic Buck Regulator Topology

The operation of this regulator topology has two distinct time periods. The first one occurs when the switch is on for the time duration DT_S, the switch conducts the inductor current and the diode becomes reverse biased. This results in a positive voltage $V_L = V_I - V_O$ across the inductor. This voltage causes a linear increase in the inductor current I_L. During this "ON" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to supply the requirements of the load during the "OFF" period.



Switch On for the Time Duration DT_S

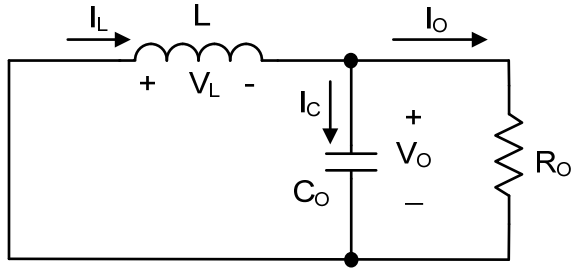


Figure B3. Switch Off For the Time Duration (1-D) T_S

The next period is the "OFF" period of the power switch. When the switch is turned off, the voltage across the inductor reverses its polarity and is clamped by the diode, because of the inductive energy storage, I_L continues to flow. The current now flows through the diode, and $V_L = -V_O$ for a time duration $(1-D)T_S$ until the switch is turned on again. Equating the integral of the inductor voltage over one time period to zero yields

$$\int_0^{T_S} V_L(t)dt = \int_0^{DT_S} V_L(t)dt + \int_{DT_S}^{T_S} V_L(t)dt,$$

$$(V_I - V_O)\times DT_S + (-V_O)\times(1-D)T_S = 0$$

$$V_O = DV_I, \quad \frac{V_O}{V_I} = D$$

$(D = \frac{t_{ON}}{T_S}$ where T_S is the period of switching)

Assuming a lossless circuit $P_I = P_O$, Therefore

$$P = V_I \times I_I = V_O \times I_O, \text{ and } \frac{I_O}{I_I} = \frac{V}{V_O} = \frac{1}{D}$$

For a buck regulator, it is obvious that

$I_L = I_O$

According to the buck operating relationship between inductor and output capacitor, shown in Figure B4, The peak-to-peak inductor current ripple ΔI_L can be calculated by following equation.

$$i_L(t) = i_L(0) + \frac{1}{L}\int V_L(t)dt, \qquad (T_S = \frac{1}{f_{OSC}}, \quad \frac{V_O}{V_I} = D)$$

$$\Delta I_L = \frac{1}{L}\left[\text{Shaded area under waveform } V_L \text{ (Area A)}\right]$$

$$\Delta I_L = \frac{1}{L}(V_I - V_O)\times DT_S = \frac{1}{L}(-V_O)\times(1-D)T_S$$

$$\Delta I_L = \frac{1}{L}\times\frac{1}{f_{OSC}}\times\frac{V_O}{V_I}(V_I - V_O)$$

From ΔI_L, we can obtain I_{L_MIN} and I_{L_MAX}

$$I_{L\_MIN} = I_L - \frac{\Delta I_L}{2}$$

$$I_{L\_MAX} = I_L + \frac{\Delta I_L}{2}$$

The peak-to-peak output voltage ripple, ΔV_O

$$\Delta V_O = \Delta V_C = \frac{1}{C}\int IC(t)dt, \qquad (Q = C\times V)$$

$$\Delta V_O = \frac{1}{L}\left[\text{Shaded area under waveform } I_L \text{ (Area B)}\right]$$

$$\Delta V_O = \frac{1}{C}\times\frac{1}{2}\times\frac{T_S}{2}\times\frac{\Delta I_L}{2}$$

$$\Delta V_O = \frac{1}{8}\times\frac{1}{f_{OSC}}\times\frac{\Delta I_L}{C}$$

Component Selection for Buck Regulator

Inductor Selection (L)

The inductance (L), saturation current rating and DC resistance (DCR) of the inductor are important parameters to consider when selecting the inductor, since these parameters affect the regulator's performance and efficiency. Base on the input V_I and output voltage V_O, switching frequency f_{OSC}, and the output load current I_O, the inductance (L) can be calculated by the following equation.

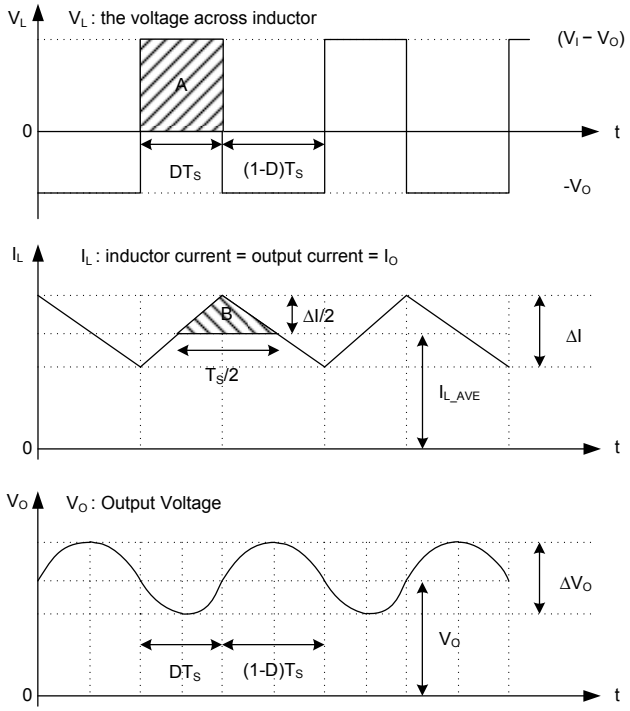


Figure B4. The operating waveform of a Buck Regulator

$$\Delta I_L = \frac{1}{L} \times \frac{1}{f_{OSC}} \times \frac{V_O}{V_I}(V_I - V_O)$$

$$L = \frac{1}{L_{IR} \times I_O} \times \frac{1}{f_{OSC}} \times \frac{V_O}{V_I}(V_I - V_O), \quad \left(L_{IR} = \frac{\Delta I}{I_O}\right)$$

Where L_{IR} is the ratio of peak to peak inductor current ripple (ΔI) to the load current I_O, and is usually set at 20%~40% of I_O. Although using a lower inductance minimizes physical size and cost, a lower inductance increases inductor current ripple and reduces the efficiency due to higher peak currents. On the other hand, a higher inductance reduces the ripple current to mitigate conduction losses and minimize output voltage ripple, but too large of an inductance leads to slow response time and lower efficiency if the losses from the higher DCR outweigh the losses eliminated from a lower ripple current.

Peak current through the inductor determines the inductor's required saturation current rating, the maximum inductor current I_{LMAX} as shown below.

$$I_{LMAX} = I_O + \frac{\Delta I_L}{2}$$

During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For these reasons, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

The DC resistance is the wire resistance of an inductor, and will result in power dissipation due to the current flowing through the inductor. Hence, the inductor DCR should be kept low for good efficiency.

Input Capacitor Selection (C_I)

The input current of the buck regulator is discontinuous, and depending on the load input peak currents can be large, causing large input voltage ripple and noise. Hence the input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current. Since the input capacitor has to absorb switching current, it requires an adequate ripple current rating. The RMS input current (I_{IRMS}) can be calculated as follows.

$$I_{IRMS} = \frac{I_O}{V_I} \times \sqrt{V_O(V_I - V_O)}$$

In the worst case, with a duty cycle of 50%,

$$D = \frac{1}{2} = \frac{V_O}{V_I}, \quad I_{I\_RMS} = \frac{I_O}{V_I} \times V_O = \frac{I_O}{2}$$

For best performance, use a low ESR input capacitor to prevent large voltage transients from appearing at the input, and to minimize power dissipation. A ceramic type capacitor is recommended because of their high RMS current rating and low ESR for a given physical dimension.

Output Capacitor Selection (C_O)

The output capacitor (C_O) functions to store energy, to maintain the output voltage, and to stabilize the regulation control system. The output capacitor is chosen to meet the output ripple specification and to provide storage for load transients. The ESR of the output capacitor and the peak–to–peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value (ΔV_O). The output ripple voltage is approximated by

$$\Delta V_O = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_O} \right)$$

For low output ripple voltage, low ESR output capacitors are recommended. When a low ESR ceramic capacitor is used, the output voltage ripple due to the ESR is small and can be ignored. In this case the output ripple is mainly attributed to the capacitor charging and discharging. Note that choosing a capacitor with very low ESR may cause the regulator system to be unstable.

The desired output voltage change during a load transient also determines the output capacitance requirement. For a given voltage change ΔV_O, and a given load change ΔI_O, the output capacitance (C_O) can be calculated by

$$C_O = \frac{L \times \left(I_O + \frac{1}{2} \Delta I_O \right)^2}{\left(\Delta V_O + V_O \right)^2 - V_O^2}$$

Where ΔI_O is the change in output current, and ΔV_O is the allowable change in the output voltage.

Rectifier Diode Selection (D)

Since the rectifier diode is a very significant source of power loss in switching power supplies, Schottky diodes are recommended for most application because of their fast recovery time and low voltage drop. Choose a rectifier with a peak voltage greater than the maximum input voltage, and the peak current rating should exceed the maximum inductor current.

Bootstrap Capacitor Selection (C_B)

A 0.1µF ceramic capacitor must be connected between the BST to LX2 pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10V or higher voltage rating.

Output Voltage Selection (V_O)

The buck output voltage is set by an external resistive voltage divider (R_{B1} and R_{B2}), and an internal reference voltage. The external resistive voltage divider feeds the dc output voltage, and an error amplifier compares it with an internal reference voltage V_{FB2} (See Figure B1). The buck output voltage can be calculated from the following equation.

$$R_{B1} = R_{B2} \times \left(\frac{V_O}{V_{FB2}} - 1 \right)$$

where V_{FB2} is 1.250V typical. If R_{B2} is chosen as 1.2 kΩ, R_{B1} is calculated to be 19.8kΩ for an output voltage of 3.3 V.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1176B.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VDD and VREF pins. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VDD and VREF bypass capacitor should referenced to analog ground (GND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost regulator contains the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node SW. The input bulk capacitance should also be placed close to these power path components to shorten the power ground length between the input and output.

Feedback and Compensation Components

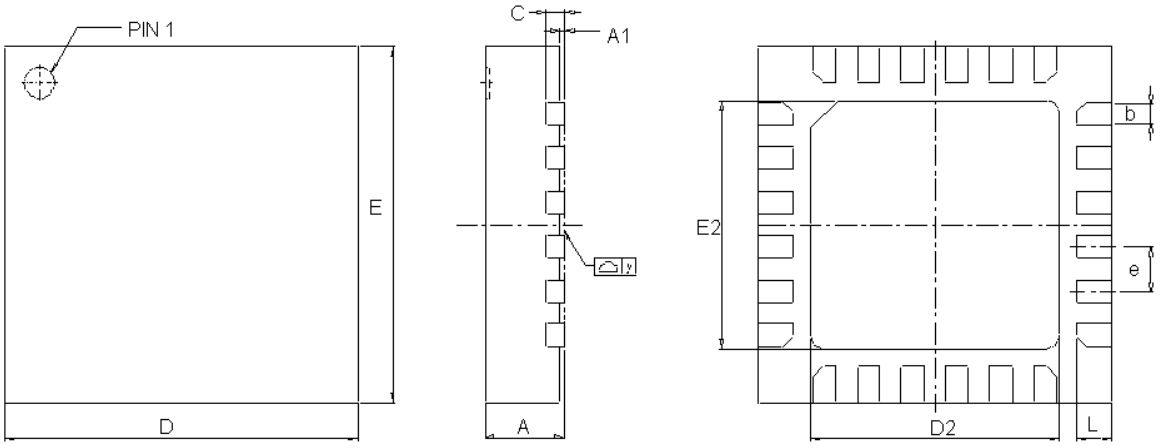
Any components for feedback, such as the resistive divider networks for setting the output voltage, should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise pickup. Likewise, compensation components should be place as close as possible to the pin or device.

Ground Plane

Use a power ground plane for the boost output capacitor ground, for the boost input bulk capacitor ground, charge pump output capacitor grounds, and GND1, GND2 pins. All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create an analog ground plane (GND) for VDD and VREF bypass capacitor grounds, compensation component ground, feedback resistive network grounds, DLY capacitor ground, RSTIN ground reference, and also the GND pins. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (GND) and power ground (GND1, GND2) should be connected only at one signal point, near the expose pad by shorting the GND pin to the expose pad.

PACKAGE DIMENSION

VQFN24-4x4x0.9mm



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
C	0.19	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	------	0.50	------
L	0.30	0.40	0.50
y	0.00	-----	0.076