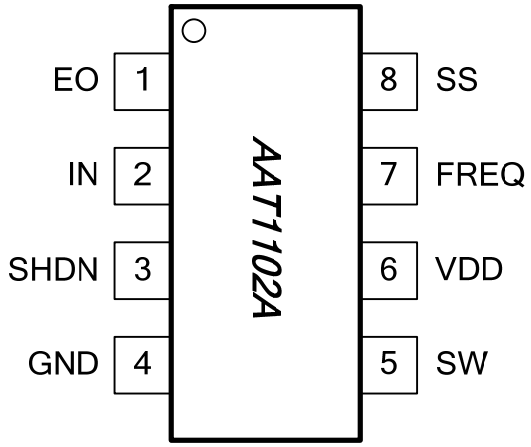
ADVANCED PWM DC-DC CONVERTER

WITH INTERNAL SWITCH AND SOFT START

FEATURES

- **2.6V to 5.5V Input Supply Voltage Range**
- **640kHz/1.3MHz Selectable Frequency**
- **Current Mode Boost Regulator**
  - **Built-in 16V, 1.6A, 0.23Ω N-MOSFET**
  - **Fast Load Transient Response**
  - **90% High Efficiency**
- **Programmable Soft Start**
- **0.1μA Shutdown Current**
- **MSOP-8 Package Available**

PIN CONFIGURATION



GENERAL DESCRIPTION

The AAT1102A is a step-up DC-DC converter with a current mode boost regulator which provides a fast transient response supply voltage. It provides an output voltage up to 16V from input voltages ranging from 2.6V to 5.5V. The boost regulator integrates a low R_{DSON} (0.23Ω) N-MOSFET, and operates at a selectable switching frequency of either 640kHz or 1.3MHz, thereby minimizing board space while providing good efficiency. An externally programmed soft start minimizes inrush current and output overshoot. In shutdown mode, current consumption is reduced to 0.1μA.

High switching frequency and economical design allows AAT1102A to be less than 1.1mm high. Its compact 8-pin MSOP package and superior performance makes it an ideal part for biasing TFT displays. The device is rated to operate from –40°C to +85°C ambient temperature range.

APPLICATIONS

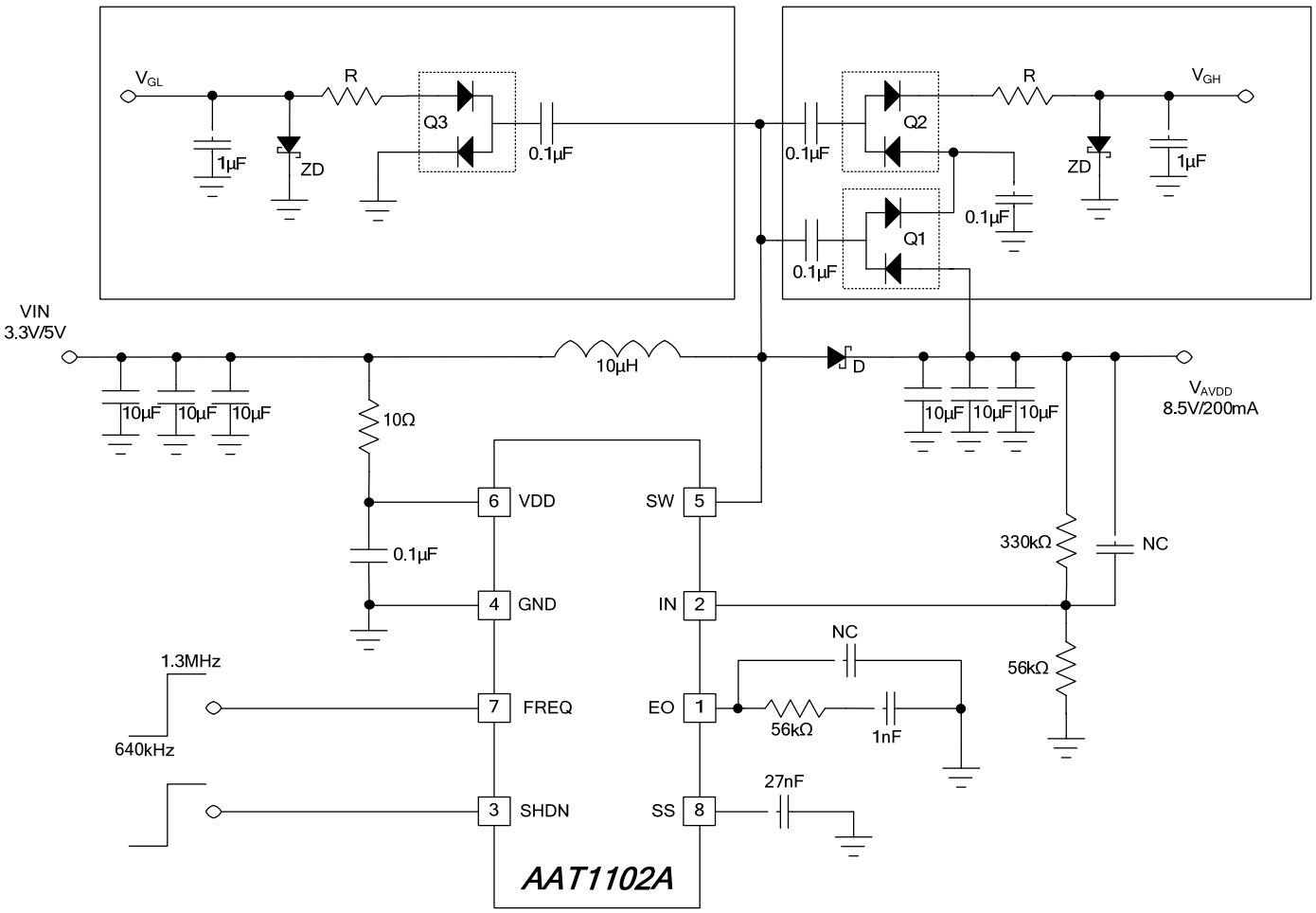
- **Smart & Notebook Panel**
- **Portable Device**

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1102A	AAT1102A-M-T	M: MSOP-8	T: Tape and Reel	–40°C to +85°C	1102A XXXX	Part Name Lot No. (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
SW to GND	V_H	–0.3 to +18	V
IN, SHDN, VDD, FREQ to GND	V_{IN}	–0.3 to +6.0	V
SS, EO to GND	V_O	–0.3V to (V_{IN} +0.3V)	V
Continuous Power Dissipation (T_C = +70°C) 8-Pin MSOP (De-Rate 4.1mW /°C above +70°C)	P_d	330	mW
Operation Temperature Range	T_C	–40 to +85	°C
Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Lead Temperature (Soldering for 10 Seconds)	T_L	+300	°C
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note: Absolute Maximum Ratings are threshold limit values that must not be exceeded. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

ELECTRICAL CHARACTERISTICS

(V_{DD} = SHDN = 3V, FREQ = GND, unless otherwise specified. Typical values are at T_C = +25°C .)

Operating Power

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Voltage Range	V_{DD}		2.6	-	5.5	V
VDD Under Voltage Lockout	UVLO	When V_{DD} is Rising, Typical Hysteresis is 40mV; SW Remains off Below this Level	2.25	2.38	2.52	V
Quiescent Current	I_{DD}	V_{IN} = 1.3V, Not Switching	-	0.21	0.35	mA
		V_{IN} = 1.0V, Switching	-	1.2	5.0	
Shutdown Current	I_{SC}	SHDN = GND	-	0.1	10.0	µA

Error Amplifier

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Feedback Voltage	V_{IN}	Level to Produce V_{EO} = 1.24V	1.222	1.240	1.258	V
VDD Input Bias Current	I_{IN}	V_{IN} = 1.24V	–40	0	+40	nA
Feedback-Voltage Line Regulation		Level to Produce V_{EO} = 1.24V, 2.6V < V_{DD} < 5.5V	-	0.05	0.15	%/mV
Transconductance	g_m	ΔI = 5µA	70	105	240	µS
Voltage Gain	A_V		-	1,400	-	V/V

Oscillator

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	f_{OSC}	FREQ = GND	540	640	740	kHz
		FREQ = V_{DD}	1,100	1,320	1,600	
Maximum Duty Cycle	D_{MAX}	FREQ = GND	79	85	92	%
		FREQ = V_{DD}	-	85	-	

ELECTRICAL CHARACTERISTICS

(V_{DD} = SHDN = 3V, FREQ = GND, unless otherwise specified. Typical values are at T_C = +25°C .)

N-Channel Switch

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit	I_{LIM}	V_{DD} = 1V Duty Cycle = 65%	1.2	1.6	2.3	A
On-Resistance	R_{ON}	I_{SW} = 1.2A	-	0.23	0.50	Ω
Leakage Current	I_{SWOFF}	V_{SW} = 15V	-	0.01	20.00	μA

Soft Start

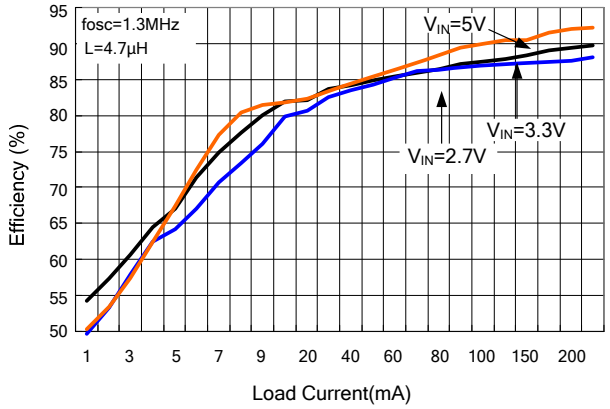
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Switch Resistance			-	-	300	Ω
Charge Current		V_{SS} = 1.2V	1.5	4.0	7.0	μA

Shutdown Control Inputs

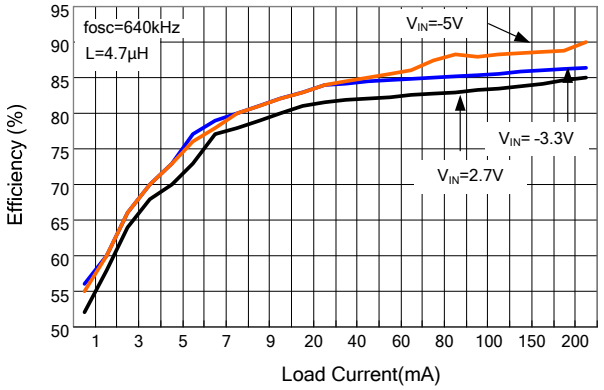
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	SHDN, FREQ V_{DD} = 2.6V to 5.5V	-	-	0.3* V_{IN}	V
Input High Voltage	V_{IH}	SHDN, FREQ V_{DD} = 2.6V to 5.5V	0.7* V_{IN}	-	-	V
Hysteresis		SHDN, FREQ	-	0.1* V_{IN}	-	V
FREQ Pull-Down Current	I_{FREQ}		1.8	5.0	9.0	μA
SHDN Input Current	I_{SHDN}		-	0.001	1.000	μA

TYPICAL OPERATING CHARACTERISTICS

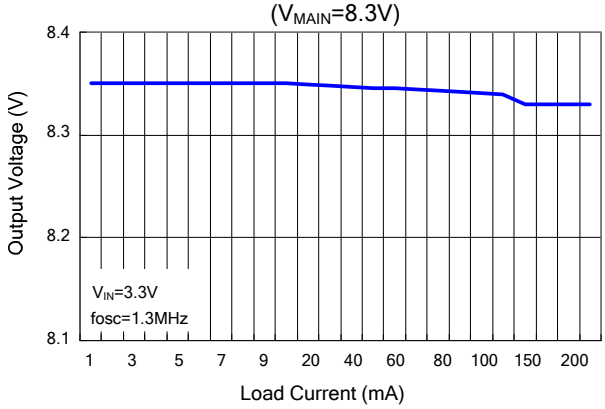
Step-up Regulator Efficiency vs. Load Current (V_{MAIN}=8.3V)



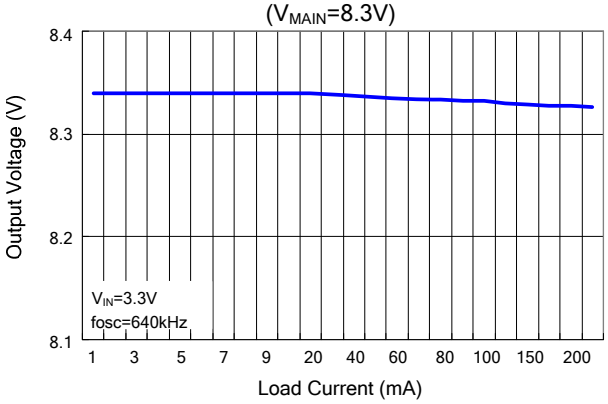
Step-up Regulator Efficiency vs. Load Current (V_{MAIN}=8.3V)



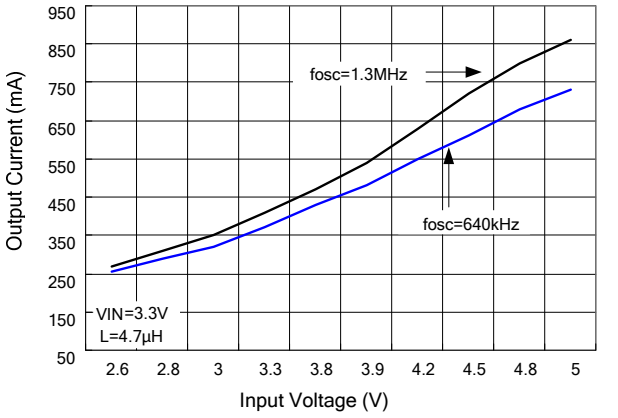
Step-up Regulator Output Voltage vs. Load Current (V_{MAIN}=8.3V)



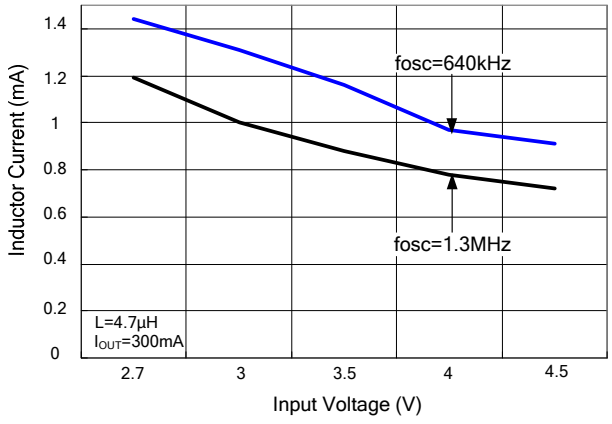
Step-up Regulator Output Voltage vs. Load Current (V_{MAIN}=8.3V)



Maximum Load Current (V_{MAIN}=8.3V) vs. Input Voltage



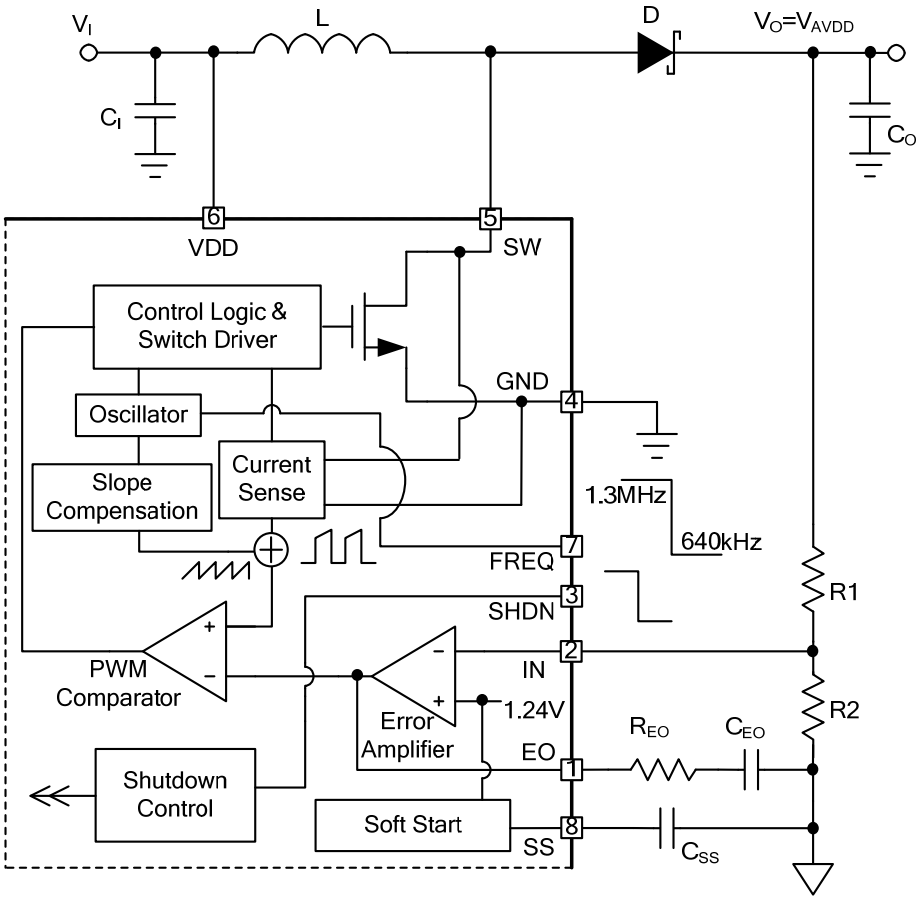
Maximum Inductor Current (V_{MAIN}=8.3V) vs. Input Voltage



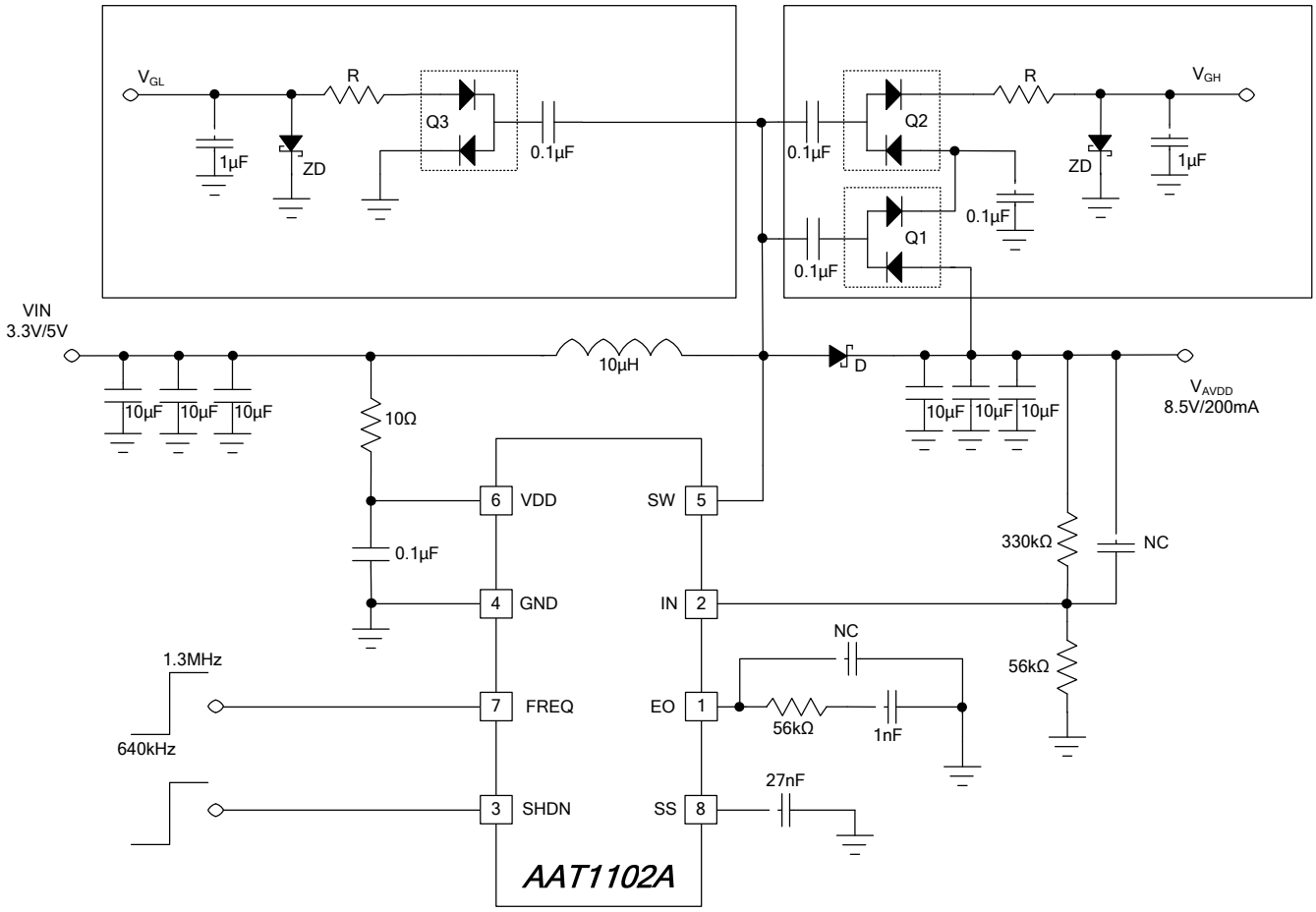
PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	EO	Compensation Pin for Error Amplifier
2	IN	Feedback Pin with a Typical Reference Voltage of 1.24V, V_O = IN x $(1+\frac{R_1}{R_2})$
3	SHDN	Shutdown Control Pin. The device will turn off when SHDN is low
4	GND	Ground
5	SW	Switch Pin
6	VDD	Power Supply Pin
7	FREQ	Frequency Select Pin. Switch oscillator frequency to 640kHz when FREQ is low, and 1.3MHz when FREQ is high
8	SS	Soft Start Control Pin. No soft start when the pin is left open

FUNCTION BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



THEORY OF OPERATION

The AAT1102A is a boost regulator with built-in N-Channel Power MOSFET. This device consists of an on-chip voltage reference, error amplifier, current sense circuit, comparator, under-voltage lockout protection, and shutdown control, adjustable switching frequency, programming soft start.

Boost Regulator

The boost regulator uses a peak current mode control scheme that provides fast output response during transients, and also simple compensation. With an integrated low R_{ON} (typical 0.23Ω) NMOS, user controlled soft start, and selectable switching frequency of either 640kHz or 1.3MHz, this boost regulator is a compact and economical solution but also provides design in flexibility. The boost regulator operates from a minimum input voltage of 2.6V, and delivers an output voltage that reaches the maximum capable duty cycle. The duty cycle (D) is calculated by

$$D = \frac{V_O - V_I}{V_O} \quad \text{or} \quad \frac{V_O}{V_I} = \frac{1}{1-D}$$

where V_O is the output of the boost regulator. Typical maximum duty cycle is approximately 90%.

At the heart of the current mode topology are two feedback loops. See the AAT1102A Boost Regulator Functional Block Diagram Figure A1. One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal power switch. The second loop monitors the boost output via a resistive divider to the IN and compares the IN voltage to an internal reference voltage of 1.24V using a transconductance error amp. Regulation is achieved by modulating the internal power switch ON time. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles above 50%. During each rising edge of the internal clock pulse, the power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

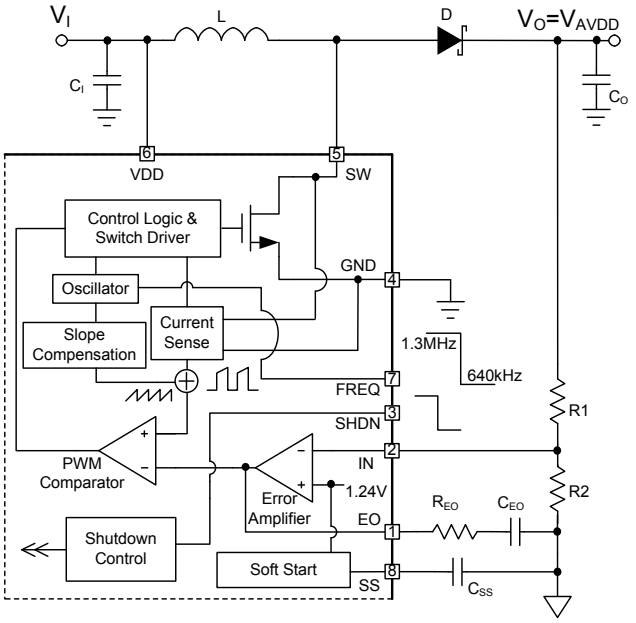


Figure A1 AAT1102A Boost Regulator Functional Block Diagram

Under Voltage Lockout (UVLO)

For systematic startup, AAT1102A employs a UVLO threshold of 2.38V. Thus, the input supply must exceed the UVLO threshold for the regulators to begin startup. Likewise, the device shuts down all functions when the input voltage is lower than UVLO falling threshold of 2.32V. A 40mV hysteresis is added to prevent device chattering when the input supply is noisy or unstable during power up or power down.

Soft Start (t_{SS}) Setting

The AAT1102A ramps up the boost regulator's current limit to achieve soft start. The soft start time is controlled via an external capacitor (C_{SS}) connected from the SS to ground. When V_I is above the UVLO threshold, an internal 4µA current source (I_{SS}) will begin to charge the capacitor from 0V to a nominal 1.24V (V_{REF}). The formula is given by

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{REF}} \quad \text{where} \quad I_{SS} = 4\mu A, V_{REF} = 1.24V$$

Operating Frequency Setting

The Boost regulator switching frequency can be set to either 640kHz or 1.3MHz. Connect FREQ to GND or leave FREQ floating for 640kHz operation. For a 1.3MHz switching frequency, connect FREQ to VDD. A higher frequency allows for smaller external filter components while maintaining low output ripple.

Shutdown Control

The AAT1102A can be disabled to reduce the supply current to 0.1µA when SHDN pin is pulled low. In this mode, the internal reference, error amplifier, comparators, and biasing circuitry turn off. The built-in NMOS is also turned off. Note that when the SHDN pin is left floating, the AAT1102A is still enabled via an internal pull-up circuit.

Thermal Control

The device enters into thermal protection shutdown when the junction temperature reaches approximately 150°C. To restart the device, the junction temperature must reduce by approximately 15°C.

APPLICATION NOTE

Boost Regulator

The AAT1102A integrates a current-mode, PWM Boost and NMOS switch. Figure A1 shows the AAT1102A Boost Regulator functional block diagram.

The boost regulator steps the input voltage up to higher output voltage. The basic configuration of a boost regulator can be seen in Figure A2.

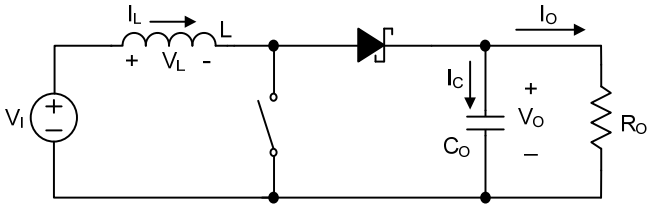
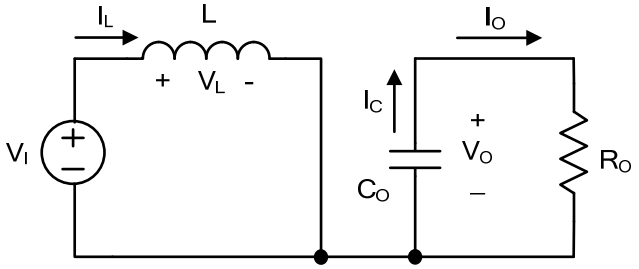


Figure A2. Basic Boost Regulator Topology

The basic boost regulator operates in two time periods. The first time duration (DT_S) occurs when the switch is on, and the diode is reversed biased. This results in a positive voltage V_L=V_I across the inductor. This voltage causes a linear increase in the inductor current I_L. During this "ON" period, energy is stored in the inductor and the load current is supplied by C_O.



Switch on for the Time Duration DT_S

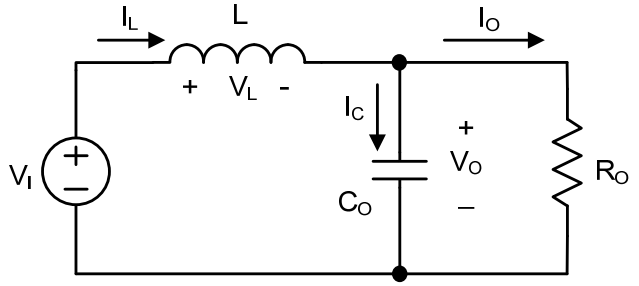


Figure A3. Switch off for the Time Duration $(1-D)T_S$

The next time duration is the "OFF" period of the power switch. When the switch is turned off, the diode is forward biased, and the energy stored in the inductor is transferred to the load and output capacitor. The voltage across the inductor reverses its polarity and is clamped by the diode, because of the inductive energy storage, I_L continues to flow. The current now flows through the diode, and $V_L = -(V_O - V_I)$ for a time duration $(1-D)T_S$ until the switch is turned on again.
Equating the integral of the inductor voltage over one time period to zero yields

$$\int_0^{T_S} V_L(t)dt = \int_0^{DT_S} V_L(t)dt + \int_{DT_S}^{T_S} V_L(t)dt,$$

$(D = \frac{t_{ON}}{T_S}$ where T_S is the period of switching)

$$V_I \times DT_S - (V_O - V_I) \times (1-D)T_S = 0$$

$$V_I = (1-D)V_O, \quad \frac{V_O}{V_I} = \frac{1}{1-D}$$

Component Selection for Boost Regulator

Inductor Selection (L)

The value of the inductor is calculated based on the input V_I and output voltage V_O, switching frequency f_{OSC}, and the nominal output load current I_O. However, when selecting the optimal inductance, both the regulator's performance and the inductor size or cost must be considered. According to the operating relationship between inductor voltage and inductor current shown in Figure A4, the Inductor ripple current (ΔI) can be calculated by the following equation.

$$iL(t) = iL(0) + \frac{1}{L}\int V_L(t)dt, \quad \left(T_S = \frac{1}{f_{OSC}}, \quad \frac{V_O}{V_I} = \frac{1}{1-D}\right)$$

$$\Delta I = \frac{1}{L} V_I \times DT_S = -\frac{1}{L}(V_O - V_I) \times (1-D)T_S$$

$$\Delta I = \frac{1}{L} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I)$$

And obtain Inductance L

$$L = \frac{1}{\Delta I} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I),$$

$$\left(\eta = \frac{V_O \times I_O}{V_I \times I_I}, \quad L_{IR} = \frac{\Delta I}{I_I} = \frac{\eta \times V_I}{V_O \times I_O} \times \Delta I\right)$$

$$L = \frac{\eta}{L_{IR}} \times \frac{1}{f_{OSC}} \times \left(\frac{V_I^2 \times (V_O - V_I)}{V_O^2 \times I_O}\right)$$

Where L_{IR} is the ratio of the ripple current (ΔI) to input current (I_I) at the full load current, and η is efficiency.
Although using a small inductance can decrease component size or cost and increase the regulator's response time, inductor ripple current increases which results in high output ripple and in lower efficiency due to increase conduction losses. Using a large inductance can lower ripple current to mitigate conduction losses and minimize output ripple, but too large of an inductance leads to slow response time and lower efficiency if the losses from the higher DCR outweigh the losses eliminated from lower ripple current. The inductor ripple current is usually adjusted by the system designer based on application for the desired cost and performance.

After selecting the inductance value, the inductor's saturation current rating should be chosen to exceed the inductor ripple current for the lowest input voltage V_{I_MIN} in the application.

$$I_{L\_AVE(MAX)} = \frac{V_O \times I_O}{V_{I\_MIN} \times \eta} \quad \left(\text{where } \eta = \frac{V_O \times I_O}{V_I \times I_I}\right)$$

And Inductor peak current I_{L_PEAK}

$$I_{L\_PEAK} = I_{L\_AVE(MAX)} + \frac{1}{2}\Delta I$$

$$I_{L\_PEAK} = \frac{V_O \times I_O}{V_{I\_MIN} \times \eta} + \frac{1}{2L} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I)$$

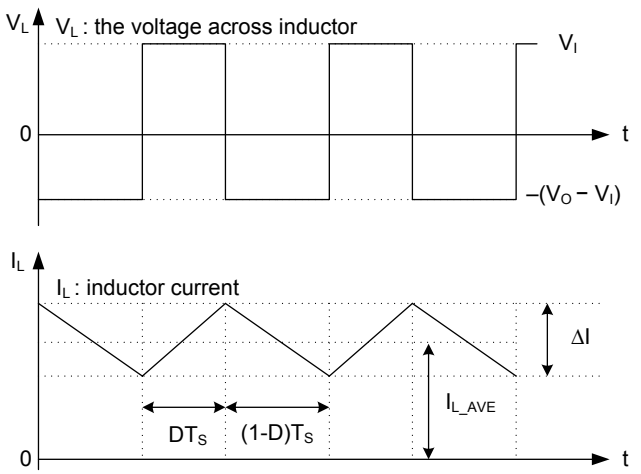


Figure A4. Inductor Voltage vs. Inductor Current (CCM)

For boost regulator, L_{IR} is usually chosen to be 0.3 to 0.5. However, if the inductor used in the TFT LCD application has significant wire resistance, higher L_{IR} (above 0.5) can be used to lower the inductance value and therefore lower the total DCR.

Output Capacitor Selection (C_O)

For switching regulators, output capacitance is chosen based on the desired output ripple and/or output voltage deviation based on a given load change.

The output voltage ripple consists of both the inductor ripple current flowing through the capacitor ESR (equivalent series resistance), and the transfer of charge to and from the output capacitor. Since in TFT LCD display applications, ceramic capacitors are used at the output, the ripple due to the IR effect can be neglected since ceramics capacitors have extremely low ESR. Thus, the ripple due to the charge and discharge of the output capacitor will be dominant. Based on a desired ripple, the minimum output capacitance can be calculated by. (Please refer to the Figure A5.)

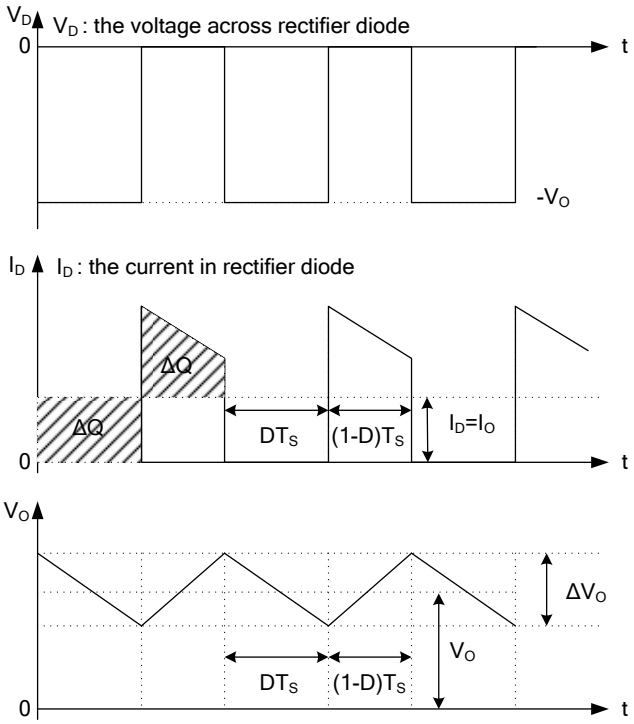


Figure A5.

$$\Delta V_O = \frac{\Delta Q}{C_O} = \frac{I_O \times DT_S}{C_O} \left(Q = CV, T_S = \frac{1}{f_{OSC}}, \frac{V_O}{V_I} = \frac{1}{1-D} \right)$$

$$\Delta V_O = \frac{I_O}{C_O} \times \frac{1}{f_{OSC}} \times \frac{(V_O - V_I)}{V_O}$$

$$C_O = \frac{I_O}{\Delta V_O} \times \frac{1}{f_{OSC}} \times \frac{(V_O - V_I)}{V_O}$$

Where ΔV_O is the output ripple voltage specification.

Note that ceramic capacitors are often used for their size advantage and environmentally-friendly nature. To achieve the required ripple or output capacitance value, multiple ceramic capacitors are often connected in parallel.

Input Capacitors Selection (C_I)

Input capacitors are usually a combination of bulk capacitor and high frequency ceramic. The bulk capacitor serves as the power source during the soft start process, supplies switching current, minimizes input ripple, and keeps the DC input voltage stable. The bulk capacitor is usually chosen to support the input RMS current, and can also be ceramic type. Often, extra bulk capacitance is added during bench evaluation to alleviate the parasitic inductance introduced from the power supply cable.

The high frequency ceramic capacitor filters the high frequency noise to the device. Usually, a 0.1µF to 1µF ceramic capacitor is used. A RC low-pass filter is often added to decrease interference from noise.

Diode Selection (D)

The diode voltage rating must be greater than the output voltage V_O and the current rating must exceed the inductor peak current I_{L_PEAK}. Using a diode with low forward voltage drop and fast recovery time to minimize the conduction loss and switching loss, and then help increase efficiency, such as a Schottky rectifier is recommended.

Output Voltage Selection (V_O)

The output voltage is set using a resistive voltage divider from the output to FB1, referenced to analog ground as shown in Figure A1. Use the following equation to set the boost voltage, or V_O,

$$R_1 = R_2 \times \left(\frac{V_O}{V_{FB1}} - 1\right)$$

Where V_{FB1} is 1.240V and R_2 = 10kΩ.

Crossover Frequency Selection

The crossover frequency, or the regulator bandwidth, is usually selected to satisfy the output step load requirement. However, due to the inherent nature of the CCM boost, a right-half-plane-zero (RHPZ) will limit the selection of the crossover frequency (f_C) due to its phase lag. A good design rule is to select the crossover frequency to be about 20% of the RHPZ frequency. The RHPZ frequency is given by

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad \text{where } R_O = \frac{V_O}{I_O}$$

$$f_C = 0.2 \times f_{RHPZ}$$

Compensation Selection (R_C & C_C)

To stabilize the boost regulator's loop, a RC series network is added from the COMP output pin to analog ground. See Figure A1, R_C is chosen to set the amplifier gain for a targeted crossover frequency. Setting the total loop gain to unity gain at the desire crossover frequency, we can calculate R_C by approximately.

$$R_C = 0.3 \times \frac{V_O}{V_{FB1}} \times \frac{V_O}{V_I} \times \frac{\pi \times f_C \times C_O}{g_m \times g_{CS}}$$

Where g_m=105µS is the feedback error amplifier transconductance, g_{CS}=4S is the current sense transconductance, the crossover frequency of the regulator f_C=20% × f_{RHPZ}, and V_{FB1} is the feedback reference voltage of 1.24V. In typical application, RC value ranges from 10kΩ to 100kΩ.

Once R_C is selected, C_C is adjusted to place a zero for neutralizing the output pole caused by the output capacitance C_O and load R_O. Use the following equation to calculate C_C,

$$C_C = \frac{C_O \times R_O}{50 \times R_C}$$

In typical application, C_C value ranges from 680pF to 2.2nF.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1102A.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VDD pins. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VDD bypass capacitor should referenced to analog ground (GND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost regulator contains the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node SW. The input bulk capacitance should also be placed close to these power path components to shorten the power ground length between the input and output.

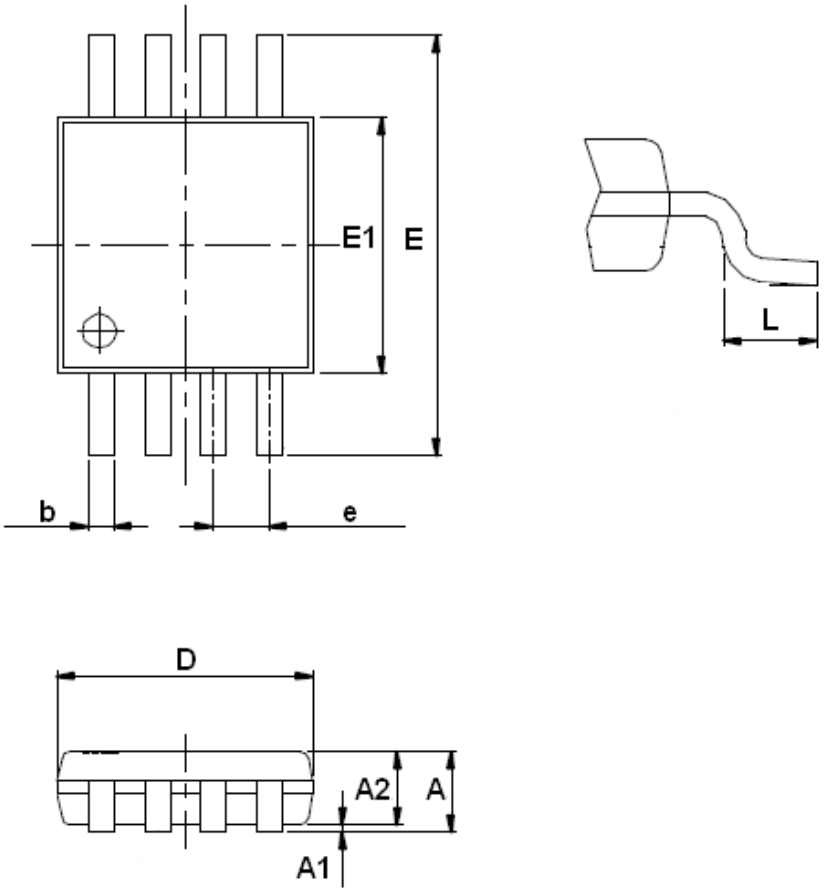
Feedback and Compensation Components

Any components for feedback, such as the resistive divider networks for setting the output voltage, should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise pickup. Likewise, compensation components should be place as close as possible to the pin or device.

Ground Plane

Use a power ground plane for the boost output capacitor ground, for the boost input bulk capacitor ground, positive charge pump output capacitor grounds, and PGND pin. All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. The power ground plane is usually a plane of copper on the component side of the PCB. Using an internal layer of the PCB, create an analog ground plane for the input bypass capacitor ground, compensation component ground, feedback resistive network ground. Analog ground plane and power ground plane should be connected via multiple vias.

PACKAGE DIMENSION



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.8	------	1.1
A1	0	------	0.15
A2	0.75	0.85	0.95
b	0.22	------	0.38
D	2.9	3.0	3.1
E	4.8	4.9	5.0
E1	2.9	3.0	3.1
e	0.55	0.65	0.75
L	0.4	0.6	0.8