MULTI-CHANNEL POWER SUPPLY FOR TFT LCD PANELS

FULLY I2C INTERFACE CONTROL – BOOST, THREE BUCKS, TWO CHARGE PUMP, GATE PULSE MODULATION

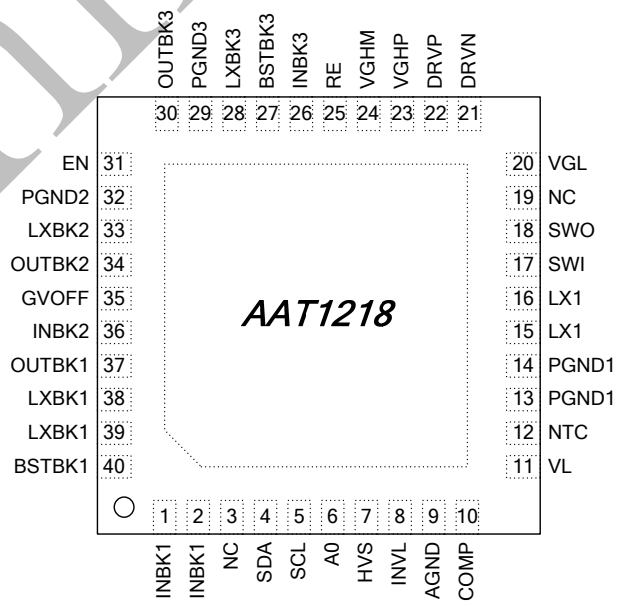
FEATURES

- 8V to 14V Input Supply Voltage Range
- Fully I^2C Interface Control
- Current Mode Boost Regulator for V_{AVDD}
  - Built-in 20V, 5A, 0.2Ω MOSFET
  - 750kHz Fixed Switching Frequency
  - Built-in Isolation NMOS Switch
  - Built-in High Voltage Stress Function (HVS)
  - Setting via I^2C Interface :
    Output Voltage, High Voltage Stress Mode, Current Limit, and Soft Start Time
- Current Mode Buck Regulator for V_{IO}
  - Built-in 18V, 3.5A, 0.2Ω, MOSFET
  - 750kHz Fixed Switching Frequency
  - Setting via I^2C Interface : Output Voltage
- Current Mode Sync Buck Regulator for V_{CORE}
  - Built-in 5V, 3A, 0.2Ω MOSFET
  - 2MHz Fixed Switching Frequency
  - Setting via I^2C Interface : Output Voltage
- Current Mode Sync Buck Regulator for V_{HAVDD}
  - Built-in 18V, 2A, 0.2Ω MOSFET
  - 750kHz Fixed Switching Frequency
  - Setting via I^2C Interface : Output Voltage
- Positive Charge Pump Regulator for V_{GH}
  - Temperature Compensation (T/C)
  - Setting via I^2C Interface : Output Voltage
- Negative Charge Pump Regulator for V_{GL}
  - Setting via I^2C Interface : Output Voltage
- High Voltage Switch with Gate Pulse Modulation
  - Setting via I^2C Interface :
    Stop Discharge Voltage (SDV)
- Protection
  - Input Under-voltage Lockout (UVLO)
  - Overload Current Protection (OCP)
  - Over Voltage Protection (OVP)
  - Short Circuit Protection (SCP)
  - Under Voltage Protection (UVP)
  - Thermal Shutdown (OTP)
- WQFN 40-6x6x0.75 Package

APPLICATIONS

- TFT LCD TV Panel

PIN CONFIGURATION



GENERAL DESCRIPTION

The AAT1218 is a highly integrated power management IC for TFT LCD TV panels. The device consists of a current mode boost regulator, three current mode buck regulators, a positive charge pump regulator with temperature compensation, a negative charge pump regulator, and gate pulse modulation. All of output voltages are set via I^2C interface.

The current mode boost regulator provides a fast transient response supply voltage for the source drivers. It provides an output voltage of up to 19.8V from input voltages ranging from 8V to 14V. The boost regulator integrates a low R_{DSON} (0.2Ω) N-MOSFET, and operates at a fixed switching frequency of 750kHz, thereby minimizing board space while providing good efficiency. The soft-start time set via I^2C interface minimizes inrush current and output overshoot. In addition, the AAT1218 integrates a control block that can drive an internal N-Channel MOSFET to sequence power to source drivers.

The first non-synchronous current mode buck regulator (BUCK1) operates at 750kHz and typically supplies system logic power (V_{IO}). It integrates a 18V, 3.5A, 0.2Ω, power MOSFET and features built-in 3ms soft start. The second synchronous current mode buck regulator (BUCK2) operates at 2MHz and typically supplies system core power (V_{CORE}). It integrates a 5V, 3A, 0.2Ω, power MOSFET and also includes a built-in 3ms soft start. The last synchronous current mode buck regulator (BUCK3) operates at 750kHz and typically supplies half V_{AVDD} for source drivers. It integrates a 18V, 2A, 0.2Ω, power MOSFET and uses a 10ms / 20ms soft start. All of three output voltages are set via I^2C interface.

The positive charge pump regulator supplies VGH gate-on voltage, and includes a temperature compensation function for GOA (GIP) Panel. The negative charge pump regulator generates VGL supply voltage for the gate-off voltage. Both output voltages can be programmable via I^2C interface. For improving TFT LCD Non-GOA (Non-GIP) Panel's image quality, a gate pulse modulation (GPM) circuit shapes the gate-on signal. The slope of the gate-on voltage can be set by external resistor and capacitor.

The AAT1218 device includes various protection features such as UVLO, OCP, OVP, SCP, UVP and thermal shutdown.

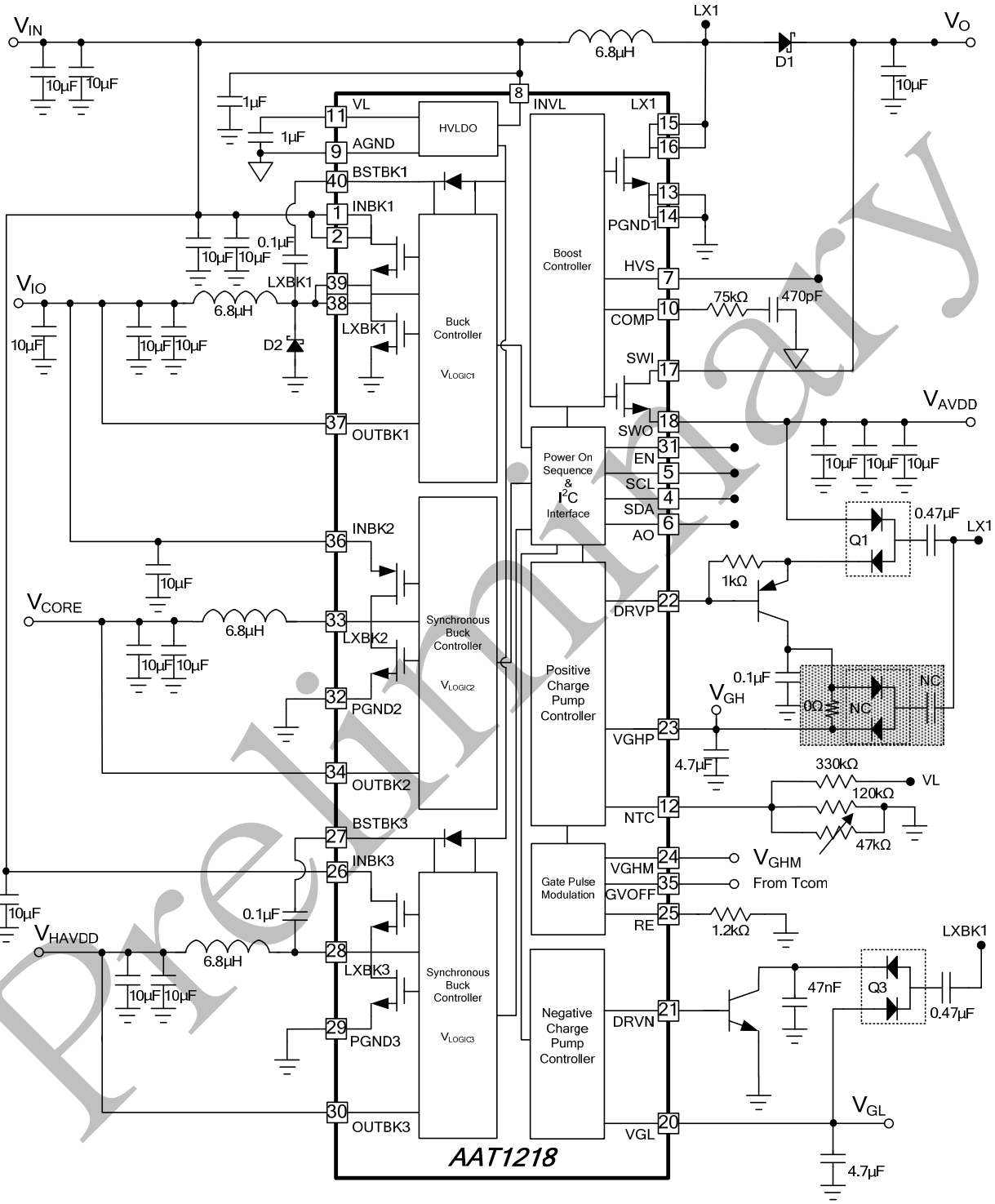
The AAT1218 is available in a small 6x6x0.75mm, ultra-thin, 40 pin WQFN package with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40°C to +85°C ambient temperature range.

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1218	AAT1218-Q23-T	Q23: WQFN40-6X6	T: Tape and Reel	–40°C to +85°C	AAT1218 XXXXXX XXXX	Device Type Lot no. (6~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
INVL , INBK1 , INBK3 to AGND	V_{IN}	–0.3 to +18	V
LX1, SWI, SWO to PGND	V_{H1}	–0.3 to +22.0	V
LXBK1, LXBK3 to PGND	V_{H2}	–0.3 to +18.0	V
INBK2, LXBK2 to PGND	V_{H3}	–0.3 to +6.0	V
BSTBK1, BSTBK3, to PGND	V_{H4}	–0.3 to +24.0	V
OUTBK1, OUTBK2 to PGND	V_O	–0.3 to +7.0	V
OUTBK3 to PGND	V_{O1}	–0.3 to +18.0	V
DRVP to PGND	V_{H5}	–0.3 to +44.0	V
DRVN to PGND	V_{H6}	–0.3 to +7.0	V
VGL to PGND	V_{H7}	–24 to –0.3	V
VGHP, VGHM, RE to PGND	V_{H8}	–0.3 to +44	V
Input Voltage (HVS, SCL, SDA, AO, NTC, GVOFF)	V_{I1}	–0.3 to +7.0	V
Input Voltage (EN)	V_{I2}	–0.3 to +18.0	V
Ourput Voltage (COMP)	V_{O2}	–0.3 to +7.0	V
Ourput Voltage (VL)	V_{O3}	–0.3 to +7.0	V
AGND to PGND (PGND1, PGND2, PGND3)	V_{I1}	–0.3 to +0.3	V
Operating Ambient Temperature Range	T_C	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Resistance	θ_{JA}	36	°C /W
Power Dissipation, @ T_C = +25°C , T_J = +125°C	P_d	2.778	W
ESD Susceptibility Human Body Mode		2k	V
ESD Susceptibility Machine Mode		200	V

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, EN = 3.3V, V_{AVDD} = 16.8V, V_{CORE} = 1.2V, $V_{I/O}$ = 3.3V, V_{HAVDD} = 8.1V, V_{GH}= 28V, V_{GL}= –10.3V)

Operating Powe

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
INVL Input Voltage Range	V_{INVL}		8	-	14	V
INVL Under Voltage Lockout	V_{UVLO}	Rising	7.0	7.2	7.5	V
		Falling	6.5	6.7	7.0	V
VL Voltage	V_L		4.90	5.00	5.10	V
EN, HVS, GVOFF Input High Voltage	V_{IH}		2	-	-	V
EN, HVS, GVOFF Input Low Voltage	V_{IL}		-	-	0.8	V
INVL Operating Current	I_{INVL}	Not Switching	-	TBD	-	mA
		Switching	-	TBD	-	mA
Thermal Shutdown	T_{SHDN}	H_{YS} = 15°C	-	150	-	°C

ELECTRICAL CHARACTERISTICS

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Non-synchronous Current Mode Boost Regulator (for AVDD)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range (SWO)	V_{AVDD}	6 Bits, Step = 0.1V	13.5	-	19.8	V
LX1 Oscillation Frequency	f_{OSC1}		600	750	900	kHz
Output Voltage Accuracy			–1	-	+1	%
LX1 Current Limit	I_{CLIM1}		4.25	5.00	5.75	A
LX1 Current Limit Negative Offset	I_{CLIM1_NO}	3 Bits, Step = 0.4A	-	-	2.8	A
LX1 NMOS ON-Resistance	R_{ON1_NMOS}		-	0.1	0.2	Ω
LX1 NMOS Leakage Current	I_{Leak1_NMOS}		-	1	20	μA
LX1 PMOS ON-Resistance	R_{ON1_PMOS}		-	0.8	-	Ω
LX1 PMOS Leakage Current	I_{Leak1_PMOS}		-	1	20	μA
LX1 Maximum Duty Cycle	D_{MAX1}		80	85	-	%
Transconductance	g_{m1}	ΔI = 5μA	-	240	-	μS
Voltage Gain	A_{V1}		-	1,000	-	V/V
Line Regulation		V_{IN} =10.8V to 13.2V, I_{AVDD} = 500mA	-	0.08	-	%/V
Load Regulation		0< I_{AVDD} < Full @ VIN = 12V	–1	-	+1	%/A
Soft Start Time	t_4	1 Bits, Step = 10ms	10	-	20	ms
Over Voltage Protect Voltage	V_{OVP_AVDD}	Hys.= 1.5V	20.5	21.5	22.5	V
Under Voltage Protect Voltage	V_{UVP_AVDD}		75	80	85	%
Duration to UVP Trigger Time	t_{UVP_AVDD}		-	50	-	ms
Short Circuit Protect Voltage	V_{SCP_AVDD}		55	60	65	%
SWO NMOS ON-Resistance	R_{ON_SWMOS}		-	0.1	0.2	Ω
High Voltage Stress (HVS) Positive Offset	HVS_{AVDD}	4 Bits, Step = 0.2V	0	-	3	V

ELECTRICAL CHARACTERISTICS

(T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, EN = 3.3V, V_{AVDD} = 16.8V, V_{CORE} = 1.2V, $V_{I/O}$ = 3.3V, V_{HAVDD} = 8.1V, V_{GH}= 28V, V_{GL}= –10.3V)

Non-synchronous Current Mode Buck Regulator (Buck1 for V_{IO})

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
INBK1 Input Voltage Range	V_{IN}		8	-	14	V
BUCK1 Output Voltage Range	V_{BUCK1}	4 Bits, Step = 0.1V	2.2	-	3.7	V
BUCK1 Output Voltage Accuracy			–2	-	+2	%
LXBK1 Oscillation Frequency	f_{OSC1}		600	750	900	kHz
LXBK1 HIGH SIDE NMOS On-Resistance	R_{ON2_HNMOS}	I_{LXBK1} = 500mA	-	0.2	-	Ω
LXBK1 HIGH SIDE NMOS Leakage Current	I_{LEAK2_HNMOS}		-	1	20	µA
LXBK1 Current Limit	I_{CLIM2}		-	3.5	-	A
Line Regulation	-	V_{IN} =10.8V to 13.2V, I_{LXBK1} = 500mA	-	0.1	-	%/V
Load Regulation	-	0 < I_{BUCK1} < 1A	-	0.5	-	%/A
Soft Start Time	t_1		-	3	-	ms
Over Voltage Protect Voltage	V_{OVP_BUCK1}		115	120	125	%
Under Voltage Protect Voltage	V_{UVP_BUCK1}		-	80	-	%
Duration to UVP Trigger Time	t_{UVP_BUCK1}		-	50	-	ms
Short Circuit Protect Voltage	V_{SCP_BUCK1}		35	40	45	%

ELECTRICAL CHARACTERISTICS

(T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, EN = 3.3V, V_{AVDD} = 16.8V, V_{CORE} = 1.2V, $V_{I/O}$ = 3.3V, V_{HAVDD} = 8.1V, V_{GH}= 28V, V_{GL}= –10.3V)

Synchronous Current Mode Buck Regulator (Buck2 for V_{CORE})

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
INBK2 Input Voltage Range	V_{INBK2}		2.2	-	3.7	V
BUCK2 Output Voltage Range	V_{BUCK2}	5 Bits, Step = 0.1V	0.8	-	3.3	V
BUCK2 Output Voltage Accuracy			–2	-	+2	%
LXBK2 Oscillation Frequency	f_{OSC2}		1.6	2.0	2.4	MHz
LXBK2 NMOS On-Resistance	R_{ON3_NMOS}	I_{LXBK2} = 500mA	-	0.2	-	Ω
LXBK2 NMOS Leakage Current	I_{LEAK3_NMOS}		-	1	20	µA
LXBK2 PMOS On-Resistance	R_{ON3_PMOS}	I_{LXBK2} = 500mA	-	0.2	-	Ω
LXBK2 PMOS Leakage Current	I_{LEAK3_PMOS}		-	1	20	µA
LXBK2 Current Limit	I_{CLIM3}		-	3	-	A
Line Regulation	-	V_{INBK2} = 2.2V to 3.7V, I_{LXBK2} = 500mA	-	0.1	-	%/V
Load Regulation	-	0 < I_{BUCK2} < 1A	-	0.5	-	%/A
Soft Start Time	t_2		-	3	-	ms
Over Voltage Protect Voltage	V_{OVP_BUCK2}		115	120	125	%
Under Voltage Protect Voltage	V_{UVP_BUCK2}		-	80	-	%
Duration to UVP Trigger Time	t_{UVP_BUCK2}		-	50	-	ms
Short Circuit Protect Voltage	V_{SCP_BUCK2}		35	40	45	%

ELECTRICAL CHARACTERISTICS

(T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, EN = 3.3V, V_{AVDD} = 16.8V, V_{CORE} = 1.2V, $V_{I/O}$ = 3.3V, V_{HAVDD} = 8.1V, V_{GH}= 28V, V_{GL}= –10.3V)

Synchronous Current Mode Buck Regulator (Buck3 for V_{HAVDD})

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
INBK3 Input Voltage Range	V_{IN}		8	-	14	V
BUCK3 Output Voltage Range	V_{BUCK3}	6 Bits, Step = 0.1V	4.8	-	11.1	V
BUCK3 Output Voltage Accuracy			–1.5	-	+1.5	%
LXBK3 Oscillation Frequency	f_{OSC1}		600	750	900	kHz
LXBK3 HIGH SIDE NMOS On-Resistance	R_{ON4_HNMOS}	I_{LXBK3} = 500mA	-	0.2	-	Ω
LXBK3 HIGH SIDE NMOS Leakage Current	I_{LEAK4_HNMOS}		-	1	20	µA
LXBK3 LOW SIDE NMOS On-Resistance	R_{ON4_LHMOS}	I_{LXBK3} = 500mA	-	0.2	-	Ω
LXBK3 LOW SIDE NMOS Leakage Current	I_{LEAK4_LNMOS}		-	1	20	µA
LXBK3 Current Limit	I_{CLIM4}		-	2	-	A
LXBK3 Maximum Duty Cycle	D_{MAX3}		80	85	-	%
Line Regulation	-	V_{IN} = 10.8V to 13.2V, I_{LXBK1} = 500mA	-	0.1	-	%/V
Load Regulation	-	0 < I_{BUCK3} < 1A	-	0.5	-	%/A
Soft Start Time	t_5	1 Bits, Step = 10ms	10	-	20	ms
Over Voltage Protect Voltage	V_{OVP_BUCK3}		115	120	125	%
Under Voltage Protect Voltage	V_{UVP_BUCK3}		-	80	-	%
Duration to UVP Trigger Time	t_{UVP_BUCK3}		-	50	-	ms
Short Circuit Protect Voltage	V_{SCP_BUCK3}		35	40	45	%

ELECTRICAL CHARACTERISTICS

(T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, EN = 3.3V, V_{AVDD} = 16.8V, V_{CORE} = 1.2V, $V_{I/O}$ = 3.3V, V_{HAVDD} = 8.1V, V_{GH}= 28V, V_{GL}= –10.3V)

Positive Charge Pump Regulator (for VGH) with Temperature Compensation

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VGH Output Voltage Range	V_{GH}	4 Bits, Step = 1V	20	-	35	V
VGH Output Voltage Accuracy			–2.5	-	+2.5	%
Output Positive Offset Voltage	V_{GH_OS}	4 Bits, Step = 1V,	-	-	15	V
VGHT Output Voltage Range	V_{GHT}	$V_{GHT} = V_{GH}+V_{GH\_OS}$	20	-	40	V
DRVP Source Current	I_{DRVP}	V_{GH} = 25V, V_{DRVP} = 18.5V	5	-	-	mA
DRVP Off-Leakage Current	I_{LEAK5}	V_{GH} = 40V, V_{DRVP} = 40V	-	0.1	10.0	µA
Soft Start Time (VGH)	t_6		-	3.0	-	ms
Over Voltage Protect Voltage	V_{OVP_VGH}		110	115	120	%
Under Voltage Protect Voltage	V_{UVP_VGH}		-	80	-	%
Duration to UVP Trigger Time	t_{UVP_VGH}		-	50	-	ms
Short Circuit Protect Voltage	V_{SCP_VGH}		35	40	45	%

High Voltage Switch with Gate Pulse Modulation (GPM)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
GVOFF Input Current	I_{Leak7}		–40	-	+40	nA
GVOFF to VGHM Propagation Delay (High to Low)	t_{PD_HL}	GVOFF H>L Transition RE = 100Ω to Ground, VGHM:10pF	-	0.25	-	µs
GVOFF to VGHM Propagation Delay (Low to High)	t_{PD_LH}	GVOFF L>H Transition RE = 100Ω to Ground, VGHM:10pF	-	0.25	-	µs
VGHM to VGHP Switch On-Resistance	R_{ON_P5}	I_{VGHM} = 20mA	-	3	5	Ω
VGHM to RE Switch On-Resistance	R_{ON_P6}	I_{RE} = 20mA	-	3	5	Ω
Stop Discharge Voltage (SDV) Negative Offset to VGH	V_{SDV_OS}	2 Bits, Step=5V SDV=V_{GH}-V_{SDV_OS}	-	-	15	V

ELECTRICAL CHARACTERISTICS

(T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, EN = 3.3V, V_{AVDD} = 16.8V, V_{CORE} = 1.2V, $V_{I/O}$ = 3.3V, V_{HAVDD} = 8.1V, V_{GH}= 28V, V_{GL}= –10.3V)

Negative Charge Pump Regulator (for VGL)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range	V_{VGL}	4 Bits, Step=-0.6V	–14.5	-	–5.5	V
VGL Output Voltage Accuracy			–2.5	-	+2.5	%
DRVN Source Current	I_{DRVN}		5	-	-	mA
DRVN Off-Leakage Current	I_{LEAK6}	V_{GL} = –11.3V, V_{DRVN} = 0V	-	0.1	10.0	µA
Soft Start (VGL)	t_3		-	3.0	-	ms
Over Voltage Protect Voltage	V_{OVP_VGL}		110	115	120	%
Under Voltage Protect Voltage	V_{UVP_VGL}		75	80	85	%
Duration to UVP Trigger Time	t_{UVP_VGL}		-	50	-	ms
Short Circuit Protect Voltage	V_{SCP_VGL}		35	40	45	%

ELECTRICAL CHARACTERISTICS

(T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, EN = 3.3V, V_{AVDD} = 16.8V, V_{CORE} = 1.2V, $V_{I/O}$ = 3.3V, V_{HAVDD} = 8.1V, V_{GH}= 28V, V_{GL}= –10.3V)

I²C Interface

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input High Voltage	V_{IH2}		1.5	-	-	V
SCL, SDA Input Low Voltage	V_{IL2}		-	-	0.6	V
SCL, SDA Input Capacitance	C_{SI}		-	5p	-	F
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA	-	-	0.4	V
SCL Clock Frequency	f_{OSCI2C}		-	-	400k	Hz
SCL Clock High Period	t_{IH3}		0.6	-	-	µs
SCL Clock Low Period	t_{IL3}		1.3	-	-	µs
SCL, SDA Receiving Rise Time	t_{R1}		-	20+0.1 *C_B	300	ns
SCL, SDA Receiving Fall Time	t_{F1}		-	20+0.1 *C_B	300	ns
I²C Data Setup Time	t_{S1}		100	-	-	ns
I²C Data Hold Time	t_{H1}		0	-	900	ns
I²C Setup Time for START Condition	t_{S2}		0.6	-	-	µs
I²C Hold Time for START Condition	t_{H2}		0.6	-	-	µs
I²C Bus Free Time Between STOP and START Conditions	t_{BUS}		4.7	-	-	µs
I²C Pulse Width of Suppressed Spike	t_{PS}		0	-	50	ns
I²C Bus Capacitance	C_B		-	-	400	pF
SDA, SCL Pull Up resistor	R_{PU}		4.7	10.0	-	kΩ

NVM

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Byte Write Time	t_{BYTE}		-	-	50	ms
Byte Read Access Time	B_{RT}		-	200	-	ns
NVM Programmable Times	N_{NVM}		-	1,000	-	Cycle

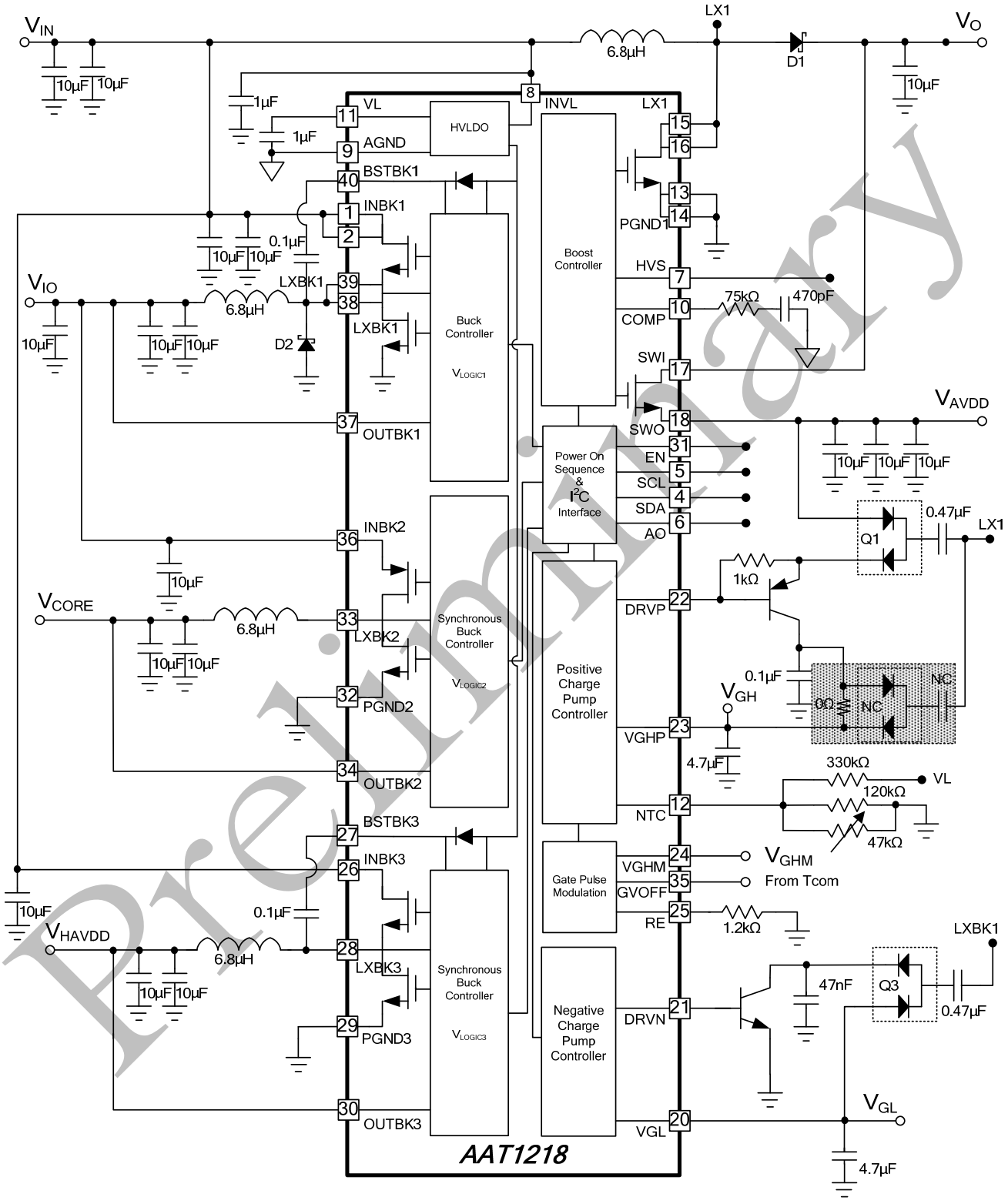
PIN DESCRIPTION

Pin No. QFN-40	Name	I/O	Description
1	INBK1	I	Buck1 PWM Power Supply Input
2	INBK1	I	Buck1 PWM Power Supply Input
3	NC	-	No Connected
4	SDA	I	I2C Serial Data Input/Output
5	SCL	I	I2C Serial Clock Input
6	A0	I	I2C Device Address Bit 0
7	HVS	I	Boost High Voltage Stress Pin
8	INVL	I	Power Supply Input
9	AGND	-	Analog Ground
10	COMP	O	Boost PWM Error Amplifier Output
11	VL	O	Internal Logic Voltage Output
12	NTC	I	Temperature Compensation Pin
13	PGND1	-	Boost PWM Power MOS Ground
14	PGND1	-	Boost PWM Power MOS Ground
15	LX1	O	Boost PWM Power MOS Switching Pin
16	LX1	O	Boost PWM Power MOS Switching Pin
17	SWI	O	Boost PWM Output
18	SWO	O	Boost PWM Output
19	NC	-	No Connected
20	VGL	O	Charge Pump VGL Output
21	DRVN	O	VGL Charge Pump Driver Output
22	DRVP	O	VGH Charge Pump Driver Output
23	VGHP	O	Charge Pump VGH Output
24	VGHM	I	Switching Gate High Voltage for TFT
25	RE	O	Gate High Voltage Fall Time Setting Pin
26	INBK3	I	Buck3 PWM Power Supply Input
27	BSTBK3	I	Gate Driver Voltage for Buck3 PWM Power MOS

PIN DESCRIPTION

Pin No. QFN-40	Name	I/O	Description
28	LXBK3	O	Buck3 PWM Power MOS Switching Pin
29	PGND3	-	Buck3 PWM Power MOS Ground
30	OUTBK3	O	Buck3 PWM Output
31	EN	I	Boost, Buck3 and VGH Enable Pin
32	PGND2	O	Buck2 PWM Power MOS Ground
33	LXBK2	O	Buck2 PWM Power MOS Switching Pin
34	OUTBK2	O	Buck2 PWM Output
35	GVOFF	I	High Voltage Switch Control Pin
36	INBK2	I	Buck2 PWM Power Supply Input
37	OUTBK1	O	Buck1 PWM Output
38	LXBK1	O	Buck1 PWM Power MOS Switching Pin
39	LXBK1	O	Buck1 PWM Power MOS Switching Pin
40	BSTBK1	O	Gate Driver Voltage for Buck1 PWM Power MOS

FUNCTIONAL BLOCK DIAGRAM



THEORY OF OPERATION

The AAT1218 offers a complete solution for powering TFT LCD panels. The device integrates three current mode buck regulators, one non-synchronous buck regulator for the IO Voltage supply, a second synchronous buck regulator for the CORE Voltage supply, and a third synchronous buck regulator for the half of AVDD voltage supply. This device also includes a boost regulator for the source driver, a positive charge pump regulator with temperature compensation to generate a gate-on voltage, a negative charge pump regulator for the gate-off voltage, and a high voltage switch with gate pulse modulation for flicker compensation. The AAT1218 features various system protection schemes such as soft start, power up sequencing, fault protection, and thermal shutdown. The I^2C interface programs various device settings such as output voltages, soft start time, etc.

Boost Regulator

The boost regulator uses a peak current mode control scheme that provides fast output response during transients, and also simple compensation. With an integrated low R_{DSON} (typical 0.2Ω) NMOS, and fixed switching frequency of 750kHz, this boost regulator is a compact and economical solution but also provides design in flexibility. The boost output voltage, current limit of power NMOS, soft start time, and high voltage stress (HVS) are programmed via I^2C interface. The output voltage can be set from 13.5V to 19.8V with a step resolution of 0.1V. The current limit of power NMOS ranges from 2.2A to 5A with 0.4A steps, soft start time can be set for either 10ms or 20ms, and the high voltage stress (HVS) can be set from 0V to 3V with 0.2V steps. The boost regulator operates from a minimum input voltage of 8V, and delivers an output voltage by modulating duty cycle D of the internal power NMOS in each switching cycle. The duty cycle is calculated by

$$D = \frac{V_O - V_I}{V_O} \quad \text{or} \quad \frac{V_O}{V_I} = \frac{1}{1-D}$$

where V_O is the output of the boost regulator.

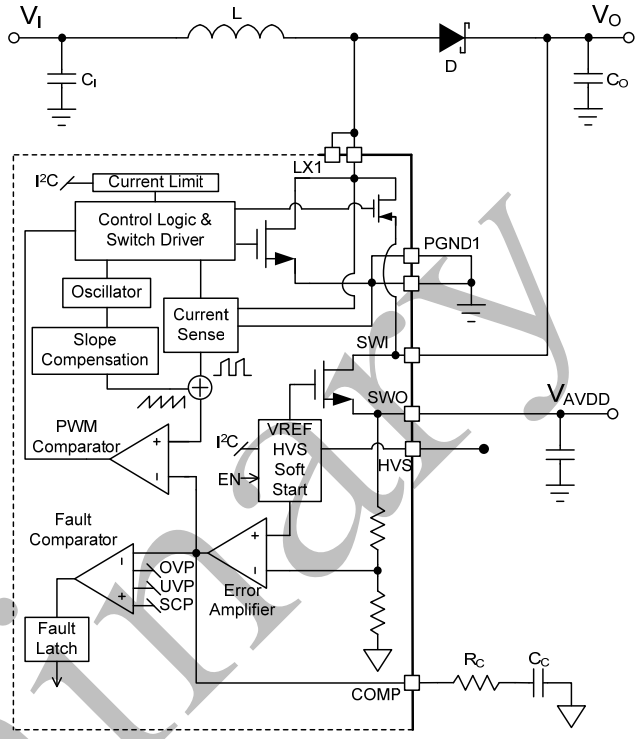


Figure 1. AAT1218 Boost Regulator Functional Block Diagram Figure

At the heart of the current mode topology are two feedback loops. See the AAT1218 Boost Regulator Functional Block Diagram Figure 1. One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal power switch. The second loop monitors the boost output via an internal feedback. This feedback voltage is compared to an internal reference voltage using a transconductance error amp. Note that the internal reference voltage is adjusted via I^2C control to set the output voltage. Regulation is achieved by modulating the internal power switch ON time. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles

above 50%. During each rising edge of the internal clock pulse, the power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

Boost Current Limit (I_{LIM1_LX1})

The boost regulator current limit can be programmed via I^2C interface, and the default current limit is 5A. The I^2C interface can reduce the current limit down from 5A to 2.2A using 3 bits with a step resolution of 0.4A. For example, setting 001 will adjust the current limit from 5A down to 4.6A.

Isolation Switch MOS Function

When EN input is high, the boost internal switch MOS between SWI and SWO will gradually turn ON within 10ms typical, allowing SWO output to become VIN. After SWO output voltage is at VIN, soft start will begin to allow for SWO to rise from VIN to its nominal value (V_{AVDD}). The soft start time can be programmed via I^2C control for either 10ms or 20ms.

High Voltage Stress Function (HVS)

HVS function increases the Boost output voltage level (V_{AVDD}). When HVS is turned ON, V_{AVDD} voltage can be increased from its nominal value via I^2C control. The I^2C control uses 4 bits with a 0.2V resolution. For example, setting the 4 bits to 1111 will results in V_{AVDD} nominal output voltage to increase by 3V. To turn on HVS function, set the HVS pin to a logic high level.

Over Voltage Protection (OVP) for AVDD

When the boost output exceeds its Over Voltage Protection threshold (typ. 21.5V), the AAT1218 disables the gate driver of this boost regulator and prevents the internal NMOS from switching. Once output voltage falls below the OVP threshold, with a hysteresis of approximately 1.5V, the boost will resume switching.

Buck Regulator (Buck1 for V_{IO})

This device integrates a non-synchronous high voltage 8V~14V input buck regulator that includes a high side low R_{DSON} (typical 0.15Ω) NMOS switch, built-in soft start of 3ms typical, 3.5A typical current limit, and internal loop compensation. An external bootstrap capacitor of 0.1µF connected from the switch node (LXBK1) to BSTBK1 is used to provide the high side gate driver supply. Note that an external Schottky diode rectifier is always required as the internal low side NMOS switch is used for charging the 0.1µF bootstrap capacitor during startup and maintains fixed frequency operation at light load.

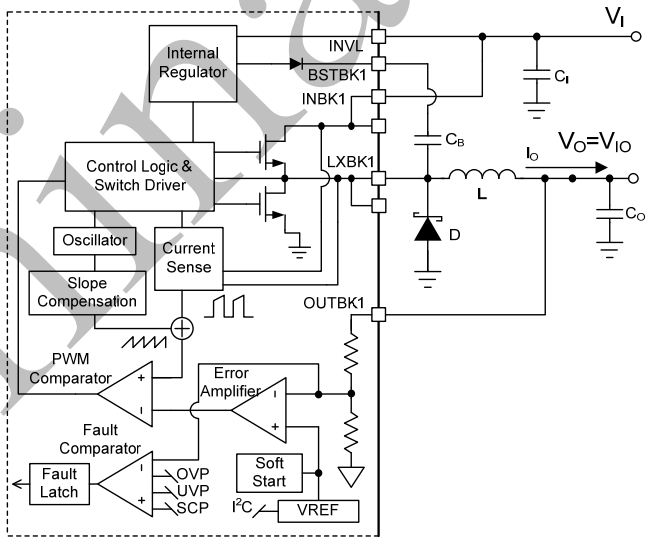


Figure 2. AAT1218 Buck1 Regulator Functional Block Diagram

The buck regulator uses the peak current mode PWM control scheme for fast transient response and cycle-by-cycle current limiting. The PWM maintains a constant frequency and varies the duty ratio according to the output voltage and load current. This modulation scheme provides high efficiency at medium to heavy load conditions, and reduces the output ripple at light load conditions. The buck output voltage can be set from 2.2V to 3.7V with a step resolution of 0.1V and operates at fixed 750kHz. The duty cycle D is calculated by

$$D = \frac{V_O}{V_I} \quad (V_O = V_{BUCK1} = V_{IO})$$

where V_O (V_{IO}) is the output voltage of the buck regulator.

In this operating mode, the high side NMOS turns on each cycle for a minimum on-time, and turns off when an internal sawtooth signal exceeds the error amplifier output which monitors the buck output via an internal feedback and compares the feedback voltage to an internal reference which is setting via I^2C control. The sawtooth signal is composed of the sensed inductor current and an artificial slope compensation ramp to prevent oscillation at duty ratios higher than 50%. After the high side NMOS is turned off, the low-side NMOS is turned on until the next cycle begins.

Buck Regulator (Buck2 for V_{CORE})

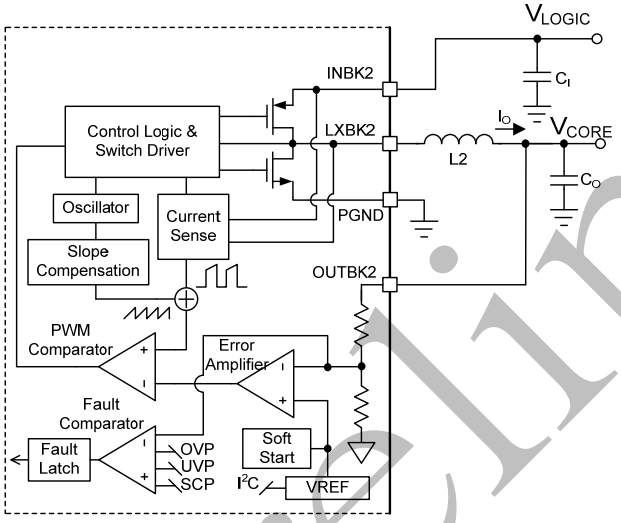


Figure 3. Buck2 Regulator Functional Block Diagram

As shown in Figure. 3, this device integrates a 2nd low voltage 2.2V~3.7V input buck regulator that includes a high-side PMOS and a low-side NMOS which eliminate the need for an external Schottky diode. Moreover, the Buck2 is compensated internally so that no external compensation network is required. Buck2 provides an output voltage of 0.8V to 3.3V, set via I2C control using a 0.1V step resolution. Current limit for Buck2 is typically 3A, and soft start is approximately 3ms. The switching frequency of Buck2 is set at 2MHz.

Buck Regulator (Buck3 for V_{HAVDD})

This device integrates a 3rd high voltage 8V~14V input buck regulator that includes a high-side NMOS and a low-side NMOS which eliminate the need for an external Schottky diode. See the AAT1218 Buck3 Regulator Functional Block Diagram Figure 4. Moreover, the Buck3 is compensated internally so that no external compensation network is required. Buck3 provides an output voltage of 4.8V to 11.1V, set via I2C control using a 0.1V step resolution. Current limit for Buc3 is typically 2A, and soft start is approximately 10 or 20ms. The switching frequency of Buck3 is set at 750kHz.

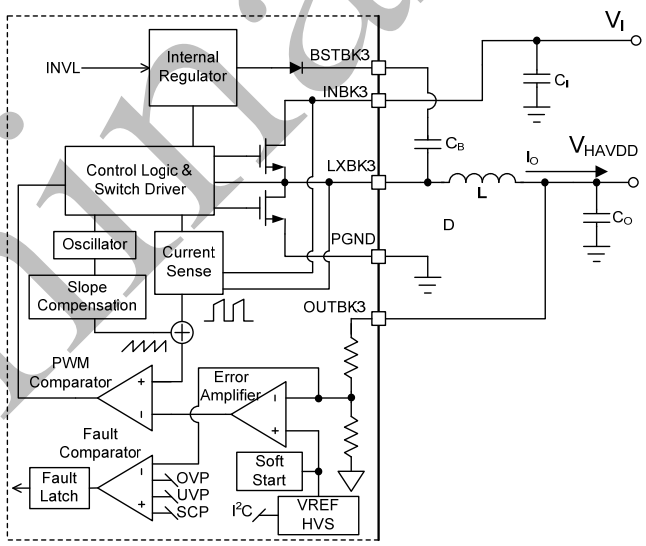


Figure 4. Buck3 Regulator Functional Block Diagram

The buck3 regulator also uses the peak current mode PWM control scheme for fast transient response and cycle-by-cycle current limiting.

Positive Charge Pump Linear Regulator Controller for VGH

The AAT1218 integrates a Charge pump linear regulator controller. This controller drives an external PNP pass transistor to form a linear regulator that receives an input voltage provided by the charge pump, and generates a linear positive supply for the TFT LCD panel gate-on voltage. For the linear regulator to

deliver the required output voltage and current, the PNP pass transistor should have proper base-to-emitter resistance to guaranteed a base-drive current. The maximum output voltage capability is determined by the number of charge pump stage, but the actual regulated output voltage is set via I^2C interface. Using a 4 bit resolution, the VGH voltage can be set from 20V to 35V. Typical application uses two stages, as shown in Figure 5.

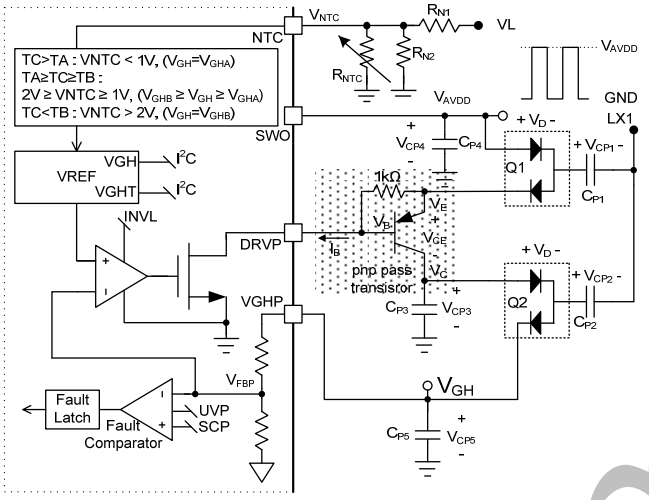


Figure 5. Positive Linear Regulator Controller Functional Block Diagram

When the LX1 is Low (GND), the flying capacitor C_{P1} and C_{P2} will charge as the higher diodes will turn on and create a path via V_{AVDD} to ground for C_{P1} and V_{CP3} to ground for C_{P2},

$V_{CP1} = V_{AVDD} - V_D$

$V_{CP2} = V_{CP3} - V_D$

V_D : the voltage drop across the diode

When the LX1 is High, pulling the charge pump operation to a high potential V_{AVDD}, and level shifting the flying capacitors. If the output capacitors are at a lower potential, by more than a diode drop than the level shifted flying capacitors, charge will flow from the flying capacitors to the output capacitors to replenish the output charge. Thus,

$V_{CP3} = V_{AVDD} + V_{CP1} - V_D - V_{CE} = 2V_{AVDD} - 2_{VD} - V_{CE}$

$V_{CP5} = V_{GH} = V_{AVDD} + V_{CP2} - V_D = V_{AVDD} + V_{CP3} - 2V_D$

Where $V_{CP2} = V_{CP3} - V_D$

$V_{GH} = 3V_{AVDD} - 4V_D - V_{CE}$

V_{CE} : the voltage drop across the PNP transistor

The voltage magnitude of V_{CE} is controlled by the drive strength of DRVP, which is a n-channel open-drain output. When the PNP pass transistor is fully turned ON, the maximum capable output of this two stages charge pump is approximately

$V_{GH} = 3V_{AVDD} - 1.4V$

Where $V_D \cong 0.3V$, $V_{CE} \cong 0.2V$

Temperature Compensation for VGH

The VGH charge pump regulator also includes temperature compensated. As shown in the functional block diagram Figure 5, the output voltage V_{GH} is compensated via the external thermistor (R_{NTC}). The voltage (V_{NTC}) at NTC Pin will adjust the reference voltage at the non-inverting input of the error amplifier. This reference voltage will also adjust the feedback regulation voltage (V_{FBP}), and therefore tune the output voltage (V_{GH}). The output voltage (V_{GH}) is compensated accordingly. For conditions where the temperature is $T_B \leqq T_C \leqq T_A$, as show in the temperature compensation for VGH Figure 6, the reference or feedback voltage (V_{FBP}) is dependent on the voltage (V_{NTC}) at the NTC Pin via the following equation:

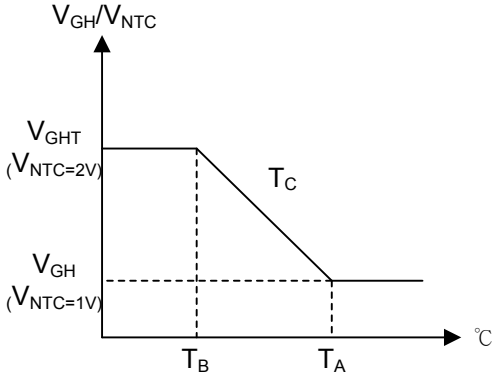


Figure 6. Temperature Compensation for VGH

$$V_{NTC} = V_L \times \left(\frac{R_{N2} \parallel R_{NTC}}{R_{N1} + (R_{N2} \parallel R_{NTC})} \right)$$

If the ambient temperature T_C is below T_B, the reference generated will be 2V. Likewise, if T_C is above T_A, the reference generated will be 1V. The conditions and equations that determine the V_{GH} voltage are summarized in Table 1.

Table 1.

°C / V	$T_C < T_B$	$T_B \leqq T_C \leqq T_A$	$T_C > T_A$
V_{NTC}	2V	V_{NTC}	1V
VGH	VGHT, I^2C Setting	Dependent on external R_{NTC} network	VGH, I^2C Setting

Negative Charge Pump Linear Regulator Controller for VGL

The AAT1218 integrates a Charge pump linear regulator controller which drives an external NPN pass transistor to form a linear regulator that receives an input voltage provided by the charge pump, and generates a linear negative supply for the TFT LCD panel gate-off voltage. For the linear regulator to deliver the required output voltage and current, an internal base-to-emitter resistance (100kΩ) for external NPN pass transistor have built in to guaranteed a base-drive current. The maximum output voltage capability is determined by the number of charge pump stage, but the actual regulated output voltage is set via I^2C interface. Using a 4 bit resolution, the VGL voltage can be set from -14.5V to -5.5V. Typical application uses a single stage, as shown in Figure 7.

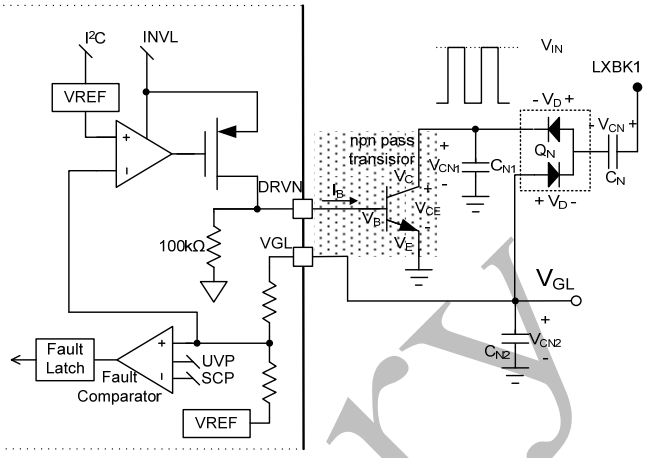


Figure 7. Negative Linear Regulator Controller Functional Block Diagram

When the LXBK1 is High (V_{IN}), the flying capacitor C_N will charge as the higher diode will turn on and create a path through NPN pass transistor to ground, and $V_{CN} = V_{IN} - V_{CE} - V_D$. When the LXBK1 is Low (GND), the flying capacitor C_N is level shifted in the negative direction, and the node connecting between C_N and Q_N becomes ($-V_{CN}$). Thus, charge will flow from the output C_{N2} to C_N, and the output can be expressed as

$$(-V_{CN}) = V_{GL} - V_D$$

$$V_{GL} = (-V_{CN}) + V_D = (-V_{IN}) + 2V_D + V_{CE}$$

The voltage magnitude of V_{CE} is controlled by the drive strength of DRVN, which is a p-channel open-drain output. When the NPN pass transistor is fully turned ON, the maximum capable output of this single stage charge pump is approximately

$$V_{GL} = (-V_{IN}) + 0.8V$$

Where $V_D \cong 0.3V$, $V_{CE} \cong 0.2V$

PASS Transistor

For the linear regulator to deliver the required output voltage and current, the NPN or PNP transistor must be properly selected. The transistor's current gain (h_{FE}) limits the guaranteed maximum output current I_C to:

$$I_C = h_{FE} \times \left(I_B - \frac{V_{BE}}{R_{BE}} \right)$$

Where I_B is the base current, V_{BE} is the bass-to-emitter

forward voltage drop, and R_{BE} is the pull-up resistor connected between the transistor's base and emitter. Note that too high of a transistor current gain can destabilize the linear regulator output due to a high loop gain.

Other factors such as the transistor saturation voltage at maximum output load current and maximum power dissipation rating of the transistor must be considered when selecting the proper NPN or PNP pass transistor.

Charge Pump Flying Capacitors

Use a 0.1µF ~ 0.47µF for the flying capacitor (C_P & C_N) and make sure that the voltage rating of the capacitor is adequate per the number of stages. The voltage rating of the capacitor must satisfy

$V_{CP} > n \times V_{AVDD}$

$V_{CN} > n \times V_{IN}$

Where V_{AVDD}/V_{IN} is the input supply to the charge pumps, and n is the number of stages per charge pump. Note that the negative charge pump uses 1 stage, i.e. n = 1.

Output Capacitors

The output capacitor of the linear regulator affects the stability of the regulator. To ensure stability, choose an output capacitor in the range of 1µF ~ 4.7µF, with low ESR.

High Voltage Switch for Gate Pulse Modulation (GPM)

An internal high voltage switch controller is included for gate pulse modulation which provides gate shaping to improve image quality in TFT LCD applications. The circuitry consist of two high voltage PMOS, one between VGHP and VGHM, and another between VGHM and RE. See Figure 8 for the Gate Pulse Modulation Functional Block Diagram. When the switch controller is enabled, logic level on the GVOFF input will determine which PMOS switch is ON or OFF. If GVOFF is logic High, P5 turns on and P6 turns off, VGHM connects to VGHP. If GVOFF is logic Low, P5 turns off and P6 turns on, VGHM connects to RE, and the V_{GHM} output is discharged via the resistor connected at RE to ground. V_{GHM} will discharge to a specified Stop Discharge Voltage (SDV) set via I^2C interface. Once the V_{GHM} reaches SDV, P6 will be turned off. Note that the resistor (R_{RE}) value can be adjusted to different discharge time or high to low transient slope rate.

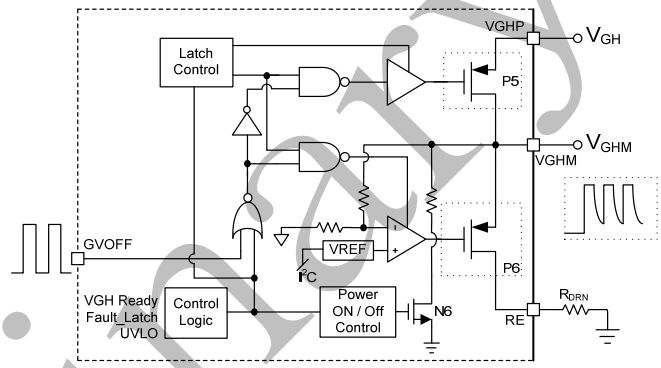


Figure 8. Gate Pulse Modulation Functional Block Diagram

The GPM must be enabled for the GVOFF input to control the PMOS switches. When the device supply voltage has exceeded the UVLO threshold, the VGHM will be pulled to ground via an internal resistor and NMOS (N6). Once the soft start has completed for V_{GH} or device is power on ready, and no fault condition is present, the NMOS switch (N6) will be turned off, the GPM will be enabled, and GVOFF will control the PMOS switches as described above.

During operation, if the input supply falls below the UVLO threshold, the GPM will be immediately disabled. Instantly, the high side PMOS P5 will turn on, the low side PMOS P6 will turn off simultaneously, and GVOFF input will have no control over the PMOS switches.

Power On/Off Sequence

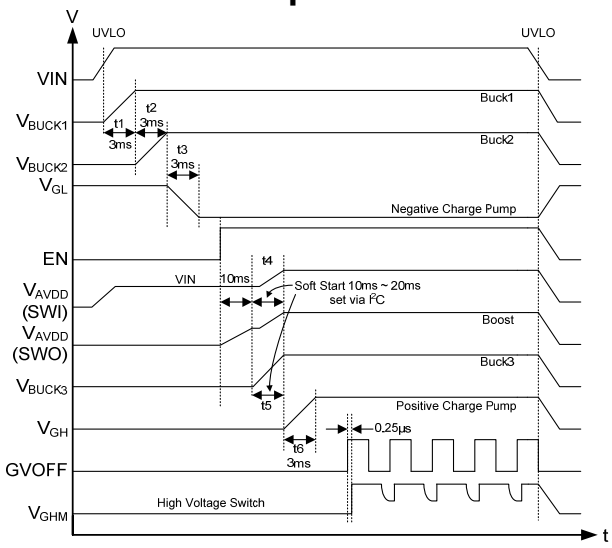


Figure 9. AAT1218 Power up Sequence

The AAT1218 Power up Sequence is as shown in Figure 9. When V_{IN} exceeds the UVLO threshold, and the internal reference (V_{REF}) is ready, the buck1 and buck2 regulators first powers up. Once the buck regulators has completed its soft start and is in regulation, the negative charge pump (V_{GL}) begins to power up. When the EN input is logic high, the boost regulator (V_{AVDD}) and buck3 will start its soft start and power up. The positive charge pump (V_{GH}) will only begin to turn on when the boost and buck3 have completed its soft start. The GPM is enabled via the GVOFF input. Note a delay time exists when GVOFF signal is applied to when VGHM starts.

For power down, when VIN falls below the UVLO threshold, all channels are disabled and the discharge rate will depend on the output loading and output capacitors. The gate pulse modulator VGHM output will be at the VGH level.

Fault Protection

Over Voltage Protection (OVP)

When VGH, or VGL output voltage exceeds its Over Voltage Protection threshold (typ. 115% of output voltage), then VGH or VGL turns off the PNP or NPN ipolar .Once the output voltage VGH or VGL falls below the OVP threshold, then turns on the bipolar again.

If either the buck1/buck2 output voltage exceeds its Over Voltage Protection threshold (typ. 120% of output voltage) , the device will shutdown all 6 channels. Moreover , if buck3 output voltage exceeds its Over Voltage Protection threshold (typ. 120% of output voltage), the device will shutdown all 4 channels (boost, buck3, VGH, or VGL).

Under Voltage Protection (UVP)

When either of the boost, buck3, VGH, or VGL output voltage drops below $0.8*V_{out}$ for more than 50ms due to overload conditions, the device will shutdown all four regulators. The buck1 and buck2 outputs will still be powered. This latched condition is reset by toggling VIN power.

If either the buck1 or buck2 output voltage drops below 0.8*Vout for more than 50ms due to overload conditions, the device will shutdown all 6 channels.

Short Circuit Protection (SCP)

When either of the boost, buck3, VGH, or VGL output voltage drops below $0.4*V_{out}$ (boost $0.6*V_{out}$)due to short circuit conditions, the device will shutdown all four channels immediately. The buck1 and buck 2 outputs will still be powered. This latched condition is reset by toggling VIN power.

If either the buck 1 or buck 2 output voltage drops below 0.4*Vout due to short circuit conditions, the device will turn off all 6 channels.

Thermal Shutdown

The AAT1218 device enters into fault protection shutdown when the junction temperature reaches

approximately 150°C. To restart the device, the junction temperature must fall below the hysteresis threshold of 15°C.

I²C Serial Interface

The AAT1218 features an I²C-compatible 2-wire serial interface consisting of SDL and SDA I/O pins. Typically the SDL and SDA are open-drain outputs that require a pull up resistor to realize high-logic levels. Pull up resistor values should be chosen to ensure that the rise and fall times are within specification. A typical value for the pull up resistors is 4.7kΩ. Each slave on the I²C bus responds to a slave address byte sent immediately following a Start Condition. Below diagram shows the timing definition for I²C interface protocol:

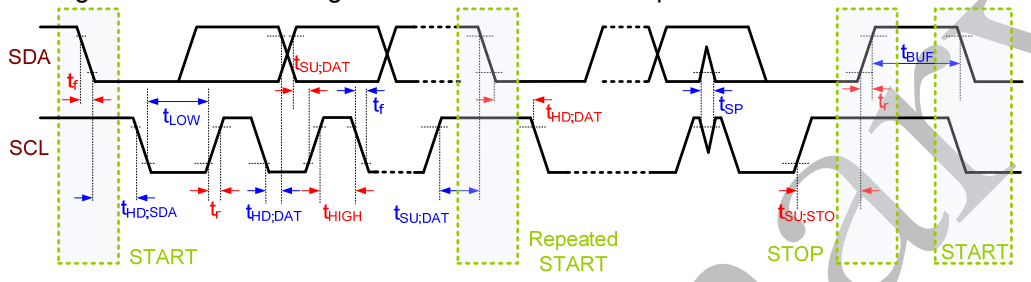


Figure 10. Definition of timing on I²C bus

The slave address byte contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit. Bit 1 can be selected depending on the address pin configuration of A0. The slave address byte of the AAT1218 is shown as following:

0	1	0	0	0	0	A0	R/$\overline{W}$

MSB LSB

Table 2 AAT1218 slave address byte

Name	Symbol	Address	Factory Value	Bit Count	Min	Max	Resolution
Channel Disable	CHN_{DIS}	00h	00h	6	-	-	-
Boost output voltage	V_{AVDD}	01h	29h (17.6V)	6	13.5V	19.8V	0.1V
Boost HVS voltage (positive offset)	HVS_{AVDD}	02h	08h (1.6V)	4	0V	3V	0.2V
Current limit value (negative offset)	I_{CLIM1}	03h	04h (1.6A)	3	0A	2.8A	0.4A
Soft start time	t_4	04h	00h (10ms)	1	10ms	20ms	10ms
Buck1 output voltage	V_{BUCK1}	05h	0Bh (3.3V)	4	2.2V	3.7V	0.1V
Buck2 output voltage	V_{BUCK2}	06h	04h (1.2V)	5	0.8V	3.3V	0.1V
Buck3 output voltage	V_{BUCK3}	07h	28h (8.8V)	6	4.8V	11.1V	0.1V
VGH_L output voltage	V_{GH}	08h	0Ah (30V)	4	20V	35V	1V
VGH_H to VGH_L offset voltage (Positive)	V_{GH_OS}	09h	06h (6V)	4	0V	15V	1V
Gate shaping lower limit voltage	V_{SDV_OS}	0Ah	01h (5V)	2	0V	15V	5V
VGL output voltage	V_{VGL}	0Bh	04h (-7.9V)	4	(-)5.5V	(-)14.5V	(-)0.6V
Memory write remain time	MRT	FEh	0Fh	4	-	-	-
Control Register	CON_{REG}	FFh	00h	8	-	-	-

Channel Disable register 00h – Factory value 00h

MSB	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	LSB
Reserved	Reserved	BK2 Enable=0 Disable=1	BK3 Enable=0 Disable=1	VGH Enable=0 Disable=1	VGL Enable=0 Disable=1	VGHM Enable=0 Disable=1	NTC Enable=0 Disable=1

MRT register FEh – Factory value 0Fh

MSB	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	LSB
Reserved	Reserved	Reserved	Reserved	1	1	1	1

*MRT register is read-only. It means that the AAT1218 uses EEPROM (not MTP/OTP).

Control register (FFH)

MSB	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	LSB
WEE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	$\overline{REE}$/RDR

*WEE =1: Write data to EEPROM.

REE/$\overline{\text{RDR}}$=1: Read data from EEPROM.

REE/$\overline{\text{RDR}}$=0: Read data from DAC register.

I²C Protocol

When the R/W bit and A0 bit are 0 (such as in 40h), the master is indicating it will write data to the slave. If R/W = 1 and A0 is 0 (41h in this case), the master is indicating it wants to read from the slave. During an I²C write operation, the master must transmit a register address to identify the memory location where the slave is to store the data. The register address is always the second byte transmitted during a write operation following the slave address byte.

During power-up, the values stored in the EE (EEPROM, nonvolatile memory) are recalled into the DR (DAC Register, volatile memory).

WRITE OPERATION

Write single byte to the DR (DAC Register):

Step 1: Master sends Start Condition.

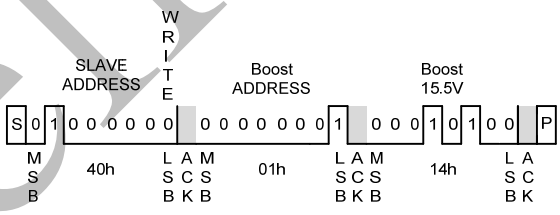
Step 2: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.

Step 3: Send DR address (ex.01h, address of Boost)
AAT1218 will acknowledge a bit for this byte

Step 4: Send the data to be written to the DR (ex.14h, Boost= 15.5V)
AAT1218 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Example: Writing 14h (15.5V) to the DR address 01h (Boost)



Write multiple bytes to the DR (DAC register):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.

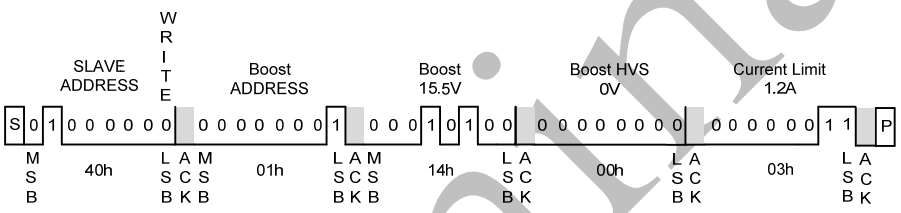
Step 3: Send DR address (ex.01h, address of Boost)
AAT1218 will acknowledge a bit for this byte

Step 4: Send the data to be written to the DR (ex.14h, Boost= 15.5V)
AAT1218will acknowledge a bit for this byte

Step 5: Master continues sending the other bytes to be written to the DRs.
AAT1218will acknowledge a bit for each byte and DR address will automatically increase

Step 6: Master sends Stop Condition.

Example: Writing 14h(15.5V), 00h(0V), 03h(1.2A) to the DR address 01h, 02h, 03h (Boost, Boost HVS, Current limit)



Write all DR (DAC Register) data to EE (EEPROM):

Step 1: Master sends Start Condition.

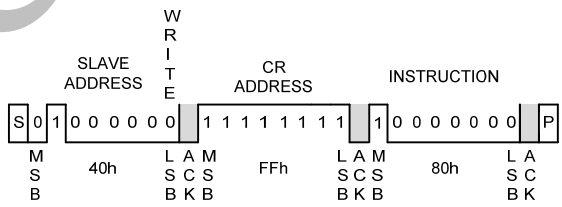
Step 2: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.

Step 3: Send CR (Control Register) address (FFh)
AAT1218 will acknowledge a bit for this byte

Step 4: Send the the value 80h to make duplicate dates from DR to EE
AAT1218 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Example: Writing all DR (00h to 0Bh) data to EE at one time.

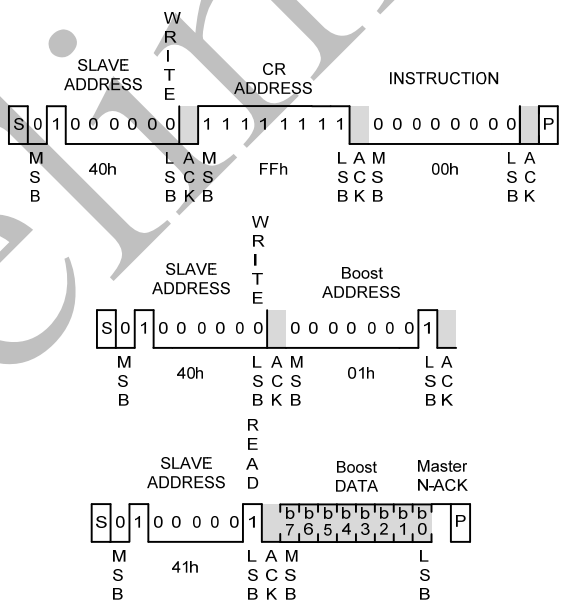


READ OPERATION

Read single data from DAC register (DR):

Step 1: Master sends Start Condition.
Step 2: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.
Step 3: Send Control Register (CR) address (FFh)
AAT1218 will acknowledge a bit for this byte
Step 4: Send the the value 00h to specify that the data is read from the DR
AAT1218 will acknowledge a bit for this byte
Step 5: Master sends Stop Condition.
Step 6: Master sends Start Condition.
Step 7: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.
Step 8: Send specified DR address to be read (ex.01h, address of Boost)
AAT1218 will acknowledge a bit for this byte
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)
Step 10: Master sends the value 41h. (the AAT1218 address 0100000b and R/W bit = High)
AAT1218 will acknowledge a bit for this byte.
Step 11: Master read the data from DR and not-acknowledges for this byte.
Step 12: Master sends Stop Condition.

Example: Reading data from the DR addresses 01h (Boost)



Read multiple data from DAC register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 40h. (the AAT1218 PMIC address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1218 will acknowledge a bit for this byte

Step 4: Send the the value 00h to specify that the data is read from the DR
AAT1218 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value 40h. (the AAT1218 PMIC address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.01h, address of Boost)
AAT1218 will acknowledge a bit for this byte

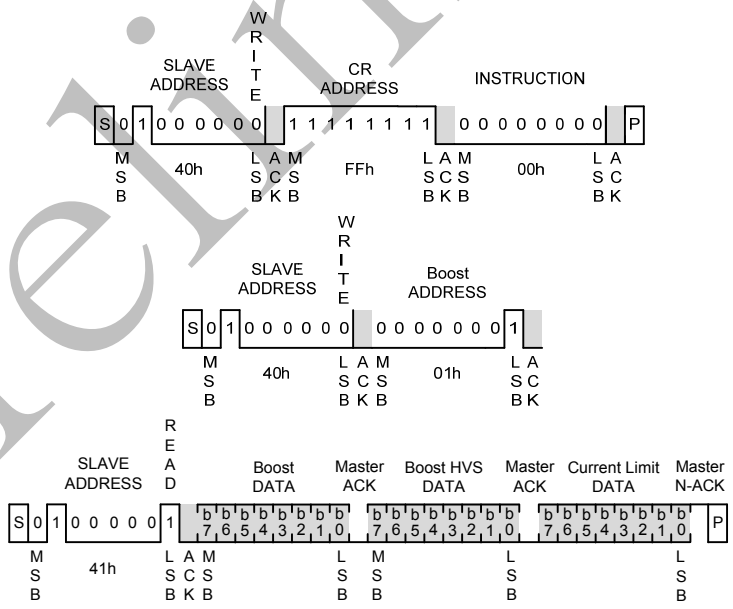
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value 41h. (the AAT1218 address 0100000b and R/W bit = High)
AAT1218 will acknowledge a bit for this byte.

Step 11: Master continues read the data from DR and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The DR address will automatically increase

Step 12: Master sends Stop Condition.

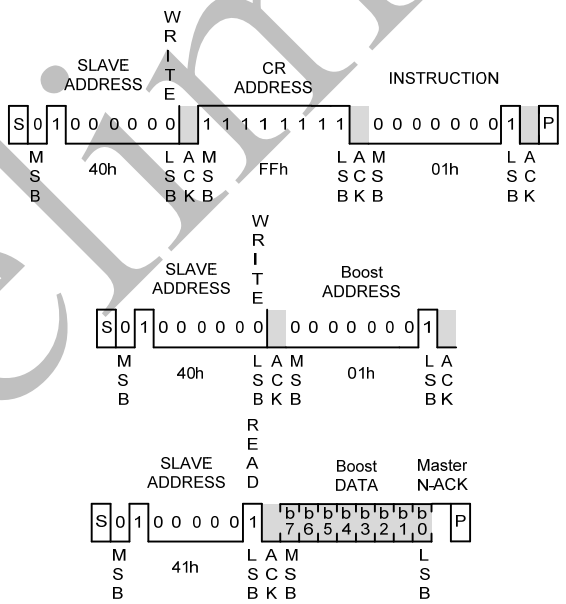
Example: Reading data from the DR addresses 01h, 02h and 03h (Boost, Boost HVS and Current Limit)



Read single data from EEPROM (EE):

Step 1: Master sends Start Condition.
Step 2: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.
Step 3: Send Control Register (CR) address (FFh)
AAT1218 will acknowledge a bit for this byte
Step 4: Send the the value 01h to specify that the data is read from the EE
AAT1218 will acknowledge a bit for this byte
Step 5: Master sends Stop Condition.
Step 6: Master sends Start Condition.
Step 7: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.
Step 8: Send specified EE address to be read (ex.01h, address of Boost)
AAT1218 will acknowledge a bit for this byte
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)
Step 10: Master sends the value 41h. (the AAT1218 address 0100000b and R/W bit = High)
AAT1218 will acknowledge a bit for this byte.
Step 11: Master read the data from EE and not-acknowledges for this byte.
Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses 01h (Boost)



Read multiple data from EEPROM (EE):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1218 will acknowledge a bit for this byte

Step 4: Send the the value 01h to specify that the data is read from the EE
AAT1218 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value 40h. (the AAT1218 address 0100000b and R/W bit = Low)
AAT1218 will acknowledge a bit for this byte.

Step 8: Send specified EE address to be read (ex.01h, address of Boost)
AAT1218 will acknowledge a bit for this byte

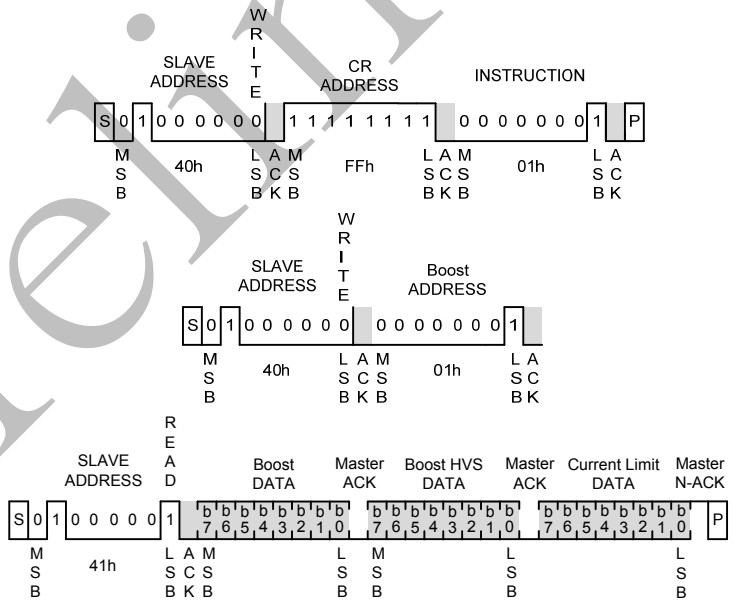
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value 41h. (the AAT1218 address 0100000b and R/W bit = High)
AAT1218 will acknowledge a bit for this byte.

Step 11: Master continues read the data from EE and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The EE address will automatically increase

Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses 01h, 02h, 03h (Boost, Boost HVS, Current Limit)



S: Start Condition, P: Stop Condition, ☐: Master to Slave, ☐:Slave to Master

length between the input and output.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1218.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VIN (INVL) pin. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VIN bypass capacitor should referenced to analog ground (AGND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost and buck regulators contain the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node LX (LX1, LXBK1, LXBK2, LXBK3). The input bulk capacitance should also be placed close to these power path components to shorten the power ground

Compensation Components

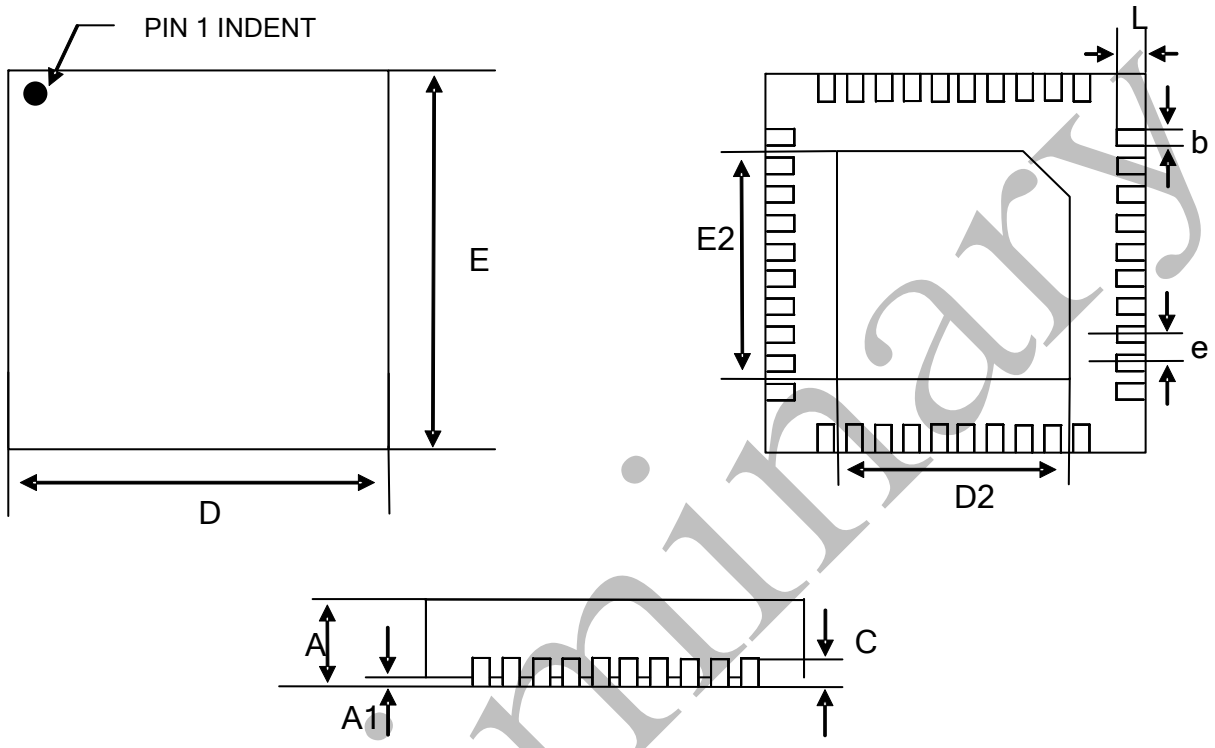
Any components for compensation components should be placed as close as possible to the pin or device. Minimize any trace length to avoid noise pickup.

Ground Plane

Use a power ground plane for the boost and buck output capacitor ground, for the boost and buck input bulk capacitor ground, charge pump output capacitor grounds, and PGND pins (PGND, PGND1, PGND2, PGND3). All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create an analog ground plane (AGND) for VIN bypass capacitor grounds, compensation component ground, feedback resistive network grounds, and also the AGND pins. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (AGND) and power ground (PGND, PGND1, PGND2, PGND3) should be connected only at one signal point, near the expose pad by shorting the AGND pin to the expose pad.

PACKAGE DIMENSION

WQFN40-6X6



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	-----	0.20	-----
D	5.90	6.00	6.10
D2	4.05	4.10	4.15
E	5.90	6.00	6.10
E2	4.05	4.10	4.15
e	-----	0.50	-----
L	0.35	0.40	0.45