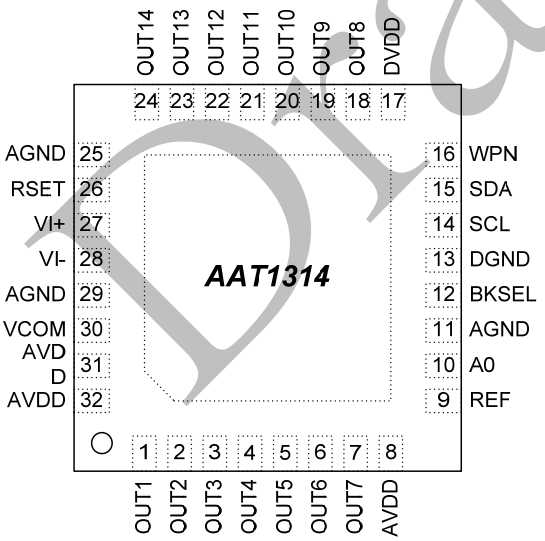
PROGRAMMABLE GAMMA AND VCOM BUFFERS

14-CHANNEL PGAMMA + 1-CHANNEL PVCOM

FEATURES

- Fully I²C Interface Control
- Input Supply Voltage Range
  - 2.3V to 3.6V Logic Supply Range
  - 6.5V to 18V Analog Supply Range
- 14-Channel Programmable Gamma Buffers
  - 10-Bit, 1024-Step Resolution
  - ±100mA Output Short Circuit
  - 10V/µs Slew Rate
  - Bank Selection
  - REF Voltage for High Accuracy DAC reference
- 1-Channel Programmable VCOM Buffer
  - 7-Bits, 128-Step Adjustable Sink Current Output
  - ±200mA Output Short Circuit
  - 20V/µs Slew Rate
- Integrated Non-Volatile Memory (NVM)
- WQFN32L-5mmx5mmx0.75mm Package Available

PIN CONFIGURATION



GENERAL DESCRIPTION

The AAT1314 provides a 14-channel programmable gamma reference and a programmable VCOM reference for applications in TFT LCD Panel. Each of the 14-channel gamma reference voltage is generated using a 10-bit digital-to-analog converter (DAC) together with a buffer via I²C control. The 14-channel gamma references support dynamic switching between two gamma curves by selecting between two different Banks of data via BKSEL select pin.

The AAT1314 also features a programmable operational amplifier that drives the LCD backplane (VCOM). This unity-gain buffer is capable of rail-to-rail input and output, ±200mA output short-circuit current, and a 20V/µs slew rate. The VCOM buffer voltage is I²C programmed using 7-bits. The digital-to-analog converter (DAC) sinks current from an external resistor-divider string to create the VCOM reference voltage, which then serves as the input to a voltage buffer capable of driving high output current.

The AAT1314 includes multiple-time programmable non-volatile memory (NVM) to store gamma and VCOM codes, eliminating the need for external EEPROM.

The AAT1314 is available in a WQFN32L-5mmx5mmx0.75mm. The device is rated to operate from –40°C to +85°C temperature range.

APPLICATIONS

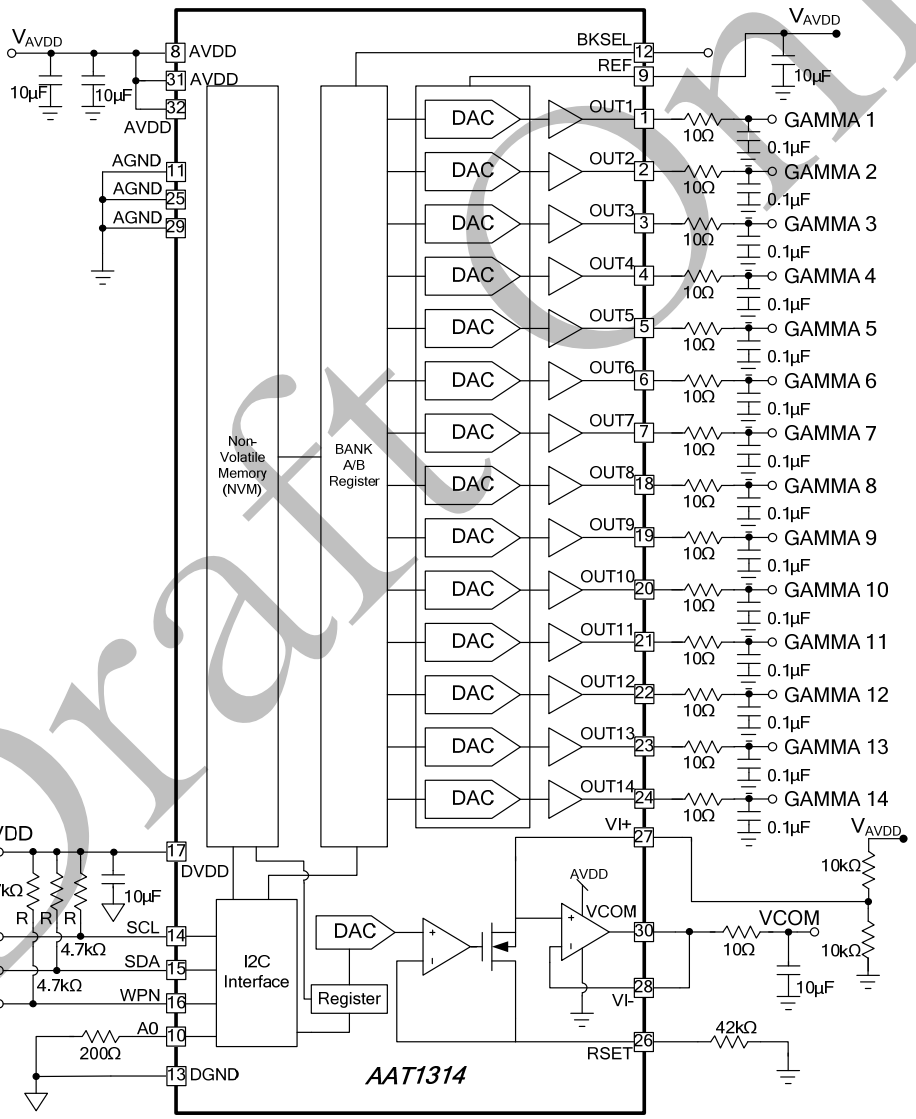
- TFT LCD Panels

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1314	AAT1314-Q29-T	Q29:WQFN 32-5*5	T: Tape and Reel	–40°C to +85°C	1314 XXXXXX XXXX	Device Type Lot no. (6~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
DVDD to DGND	V_{DVDD}	–0.3 to +7.0	V
AVDD to AGND	V_{AVDD}	–0.3 to +20.0	V
Input Voltage 1 (BKSEL, A0, SCL, SDA, WPN)	V_{I1}	–0.3 to V_{DVDD} +0.3	V
Input Voltage 2 (REF, VI+, VI–)	V_{I2}	–0.3 to V_{AVDD} +0.3	V
Output Voltage 1 (OUT1~OUT14, VCOM, RSET)	V_{O1}	–0.3 to V_{AVDD} +0.3	V
DGND to AGND	-	–0.3 to +0.3	V
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Resistance	θ_{JA}	36	°C /W
Power Dissipation, @ T_A = +25°C , T_J = +125°C	P_d	2.778	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note:
1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
2. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DVDD} = 3.3V, V_{AVDD} = REF = 16.5V, VCOM connected to VI-, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
DVDD Input Voltage Range	V_{DVDD}		2.3	-	3.6	V
DVDD Operating Current	I_{DVDD}		-	0.75	1.50	mA
DVDD Under Voltage Lockout	V_{DVDD_UVLO}		-	-	2.2	V
AVDD Input Voltage Range	V_{AVDD}		6.5	-	18.0	V
AVDD Operating Current	I_{AVDD}		-	10	15	mA
WPN Input Low Voltage	V_{WPN_L}		-	-	0.4	V
WPN Input High Voltage	V_{WPN_H}		1.4	-	-	V
WPN Input Bias Current	I_{B1}		–40	-	+40	nA
Thermal Shutdown	T_C		-	150	-	°C

ELECTRICAL CHARACTERISTICS

(V_{DVDD} = 3.3V, V_{AVDD} = REF = 16.5V, VCOM connected to VI-, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Programmable Gamma Buffers (OUT1~OUT14)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Resolution	-		10	-	-	Bits
Integral Nonlinearity Error	INL		–4	-	+4	LSB
Differential Nonlinearity Error	DNL		–1	-	+1	LSB
Full-Scale Error	SET_{FSE}	V_{AVDD} =16.5V	–4	-	+4	LSB
Output Swing	V_{GOH}	V_{AVDD} = 16.5V REF = 16.2V Code = 1013, I_{OUTx} = 5mA	Code = 1,013-30	Code = 1,013-10	-	mV
		V_{AVDD} = 16.5V REF = 16.2V Code = 512, I_{OUTx} = 30mA	Code = 512-100	Code = 512-50	100	mV
	V_{GOL}	V_{AVDD} = 16.5V REF = 16.2V Code = 512, I_{OUTx} = –30mA	-	Code = 512+50	Code = 512+100	mV
		V_{AVDD} = 16.5V REF = 16.2V Code = 10, I_{OUTx} = –5mA	-	Code = 10+10	Code = 10+10	mV
Short Circuit Current	I_{SHORT}	Output to AVDD or GND	-	±100	-	mA
Load Regulation	LR	Code = 512, I_{GOX} = 20mA & I_{GOX} = –20mA	-	±0.5	±1.5	mV/mA
Slew Rate	SR	20% to 80%	10	-	-	V/μs
Settling Time	t_S		-	5	-	μs
Power Supply Rejection Ratio	PSRR		-	60	-	dB
Bandwidth	BW		-	10	-	MHz

ELECTRICAL CHARACTERISTICS

(V_{DVDD} = 3.3V, V_{AVDD} = REF = 16.5V, VCOM connected to VI-, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Programmable VCOM Buffer

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Resolution	-		7	-	-	Bits
Integral Nonlinearity Error	INL	-	–4	-	+4	LSB
Differential Nonlinearity Error	DNL		–1	-	+1	LSB
AVDD to RSET Ratio	V_{AVDD}/R_{SET}		-	20:1	-	V/V
RSET Current	ISET	Through R_{SET}	-	-	120	µA
RSET Zero-Scale Error	$RSET_{ZSE}$		–1	+1	+2	LSB
RSET Full-Scale Error	$RSET_{FSE}$		–4	-	+4	LSB
Output Swing	V_{GOH}	V_{COM} = 3.3V I_{VCOM} = 50mA	3.20	3.25	-	V
	V_{GOL}	V_{COM} = 3.3V I_{VCOM} = –50mA	-	3.35	3.40	V
Total Output Error	E_{GOX}	Code = 512	–40	-	+40	mV
Short Circuit Current	I_{SHORT}	Measure I_{VCOM}	-	±200	-	mA
Load Regulation	LR	V_{COM} = V_{AVDD}/2 I_{VCOM} = 20mA to100mA	-	±0.5	±1.0	mV/mA
Slew Rate	SR	20% to 80%	20	25	-	V/µs
Settling Time	t_S	V_{POS} = 4.5V to 5.5V, 90%	-	5	-	µs
Power Supply Rejection Ratio	PSRR		-	60	-	dB
Bandwidth	BW		13	20	-	MHz

ELECTRICAL CHARACTERISTICS

(V_{DVDD} = 3.3V, V_{AVDD} = REF = 16.5V, VCOM connected to VI-, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

I²C Interface

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input High Voltage	V_{IH2}		1.5	-	-	V
SCL, SDA Input Low Voltage	V_{IL2}		-	-	0.6	V
SCL, SDA Input Capacitance	C_{SI}		-	5p	-	F
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA	-	-	0.4	V
SDA Output High Voltage	V_{OH}	I_{SINK} = 3mA	V_{DVDD} –0.4	-	-	V
SCL Clock Frequency	f_{OSCI2C}		-	-	400k	Hz
SCL Clock High Period	t_{IH3}		0.6	-	-	µs
SCL Clock Low Period	t_{IL3}		1.2	-	-	µs
SCL, SDA Receiving Rise Time	t_{R1}		-	20+0.1 ×C_B	300	ns
SCL, SDA Receiving Fall Time	t_{F1}		-	20+0.1 ×C_B	300	ns
I²C Data Setup Time	t_{S1}		100	-	-	ns
I²C Data Hold Time	t_{H1}		-	-	900	ns
I²C Setup Time for START Condition	t_{S2}		0.6	-	-	µs
I²C Hold Time for START Condition	t_{H2}		0.6	-	-	µs
I²C Bus Free Time Between STOP and START Conditions	t_{BUS}		4.7	-	-	µs
I²C Pulse Width of Suppressed Spike	t_{PS}		-	-	50	ns
I²C Bus Capacitance	C_B		-	-	400	pF
SDA, SCL Pull Up resistor	R_{PU}		4.7	10.0	-	kΩ

NVM

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Byte Write Time	t_{BYTE}		-	-	10	ms
Byte Read Access Time	B_{RT}		-	200	-	ns
NVM Programmable Times	N_{NVM}		-	1,000	-	Cycle

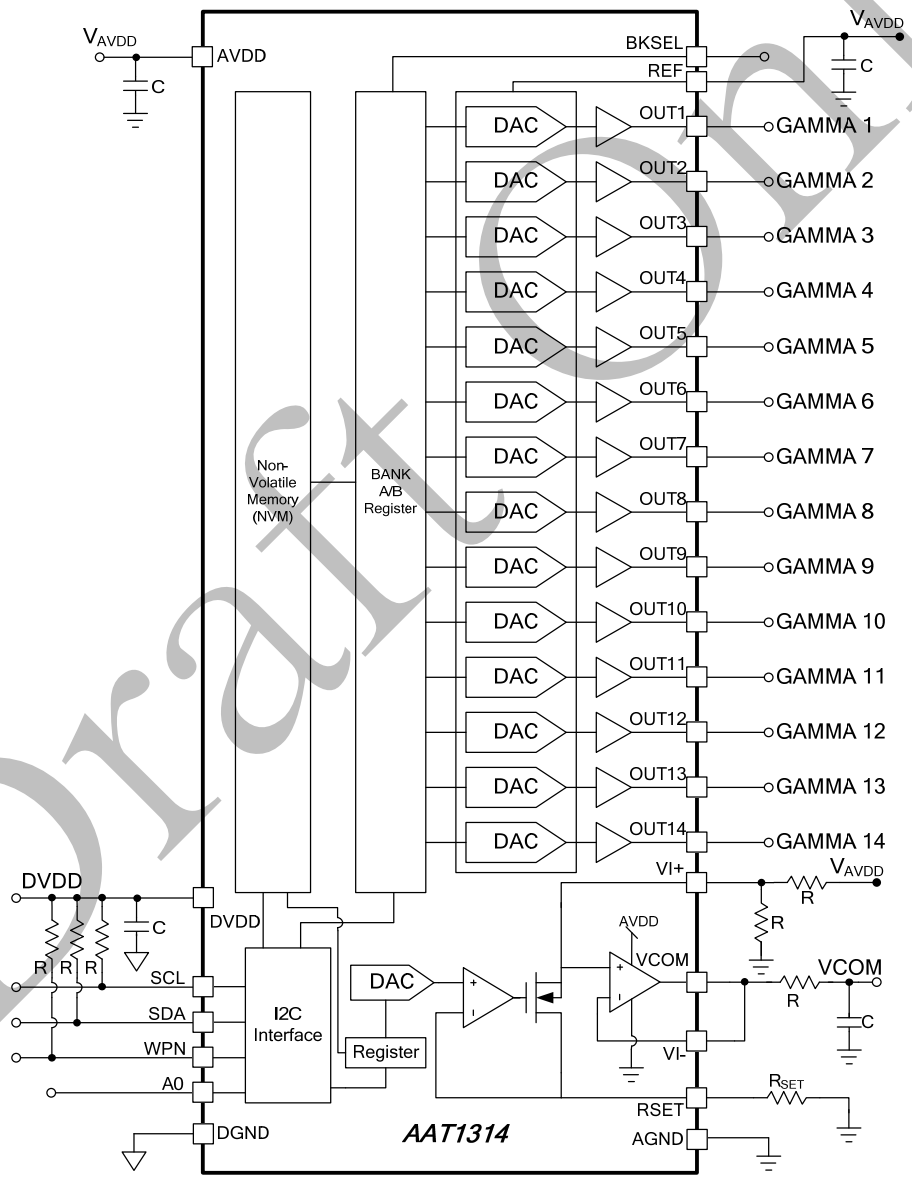
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	OUT1	O	Gamma Reference Output
2	OUT2	O	Gamma Reference Output
3	OUT3	O	Gamma Reference Output
4	OUT4	O	Gamma Reference Output
5	OUT5	O	Gamma Reference Output
6	OUT6	O	Gamma Reference Output
7	OUT7	O	Gamma Reference Output
8	AVDD	-	Analog Power Supply Input. Bypass AVDD to AGND with 10μF capacitor
9	REF	I	Reference Input for Gamma Reference Voltage
10	A0	I	Device Address Selection. Normal High (Built-in internal pull-high resister) A0 = Low : 0x74 address. A0 = High : 0x75 address
11	AGND	-	Ground of Analog Power Supply
12	BKSEL	I	Bank Selection. BKSEL = Low : BANK A. BKSEL = High : BANK B
13	DGND	-	Ground of Digital Power Supply
14	SCL	I	I^2C-Compatible Serial Clock
15	SDA	I/O	I^2C-Compatible Serial Data Input/Output
16	WPN	I	NVM Write Protection. WPN = Low: Write Enable. WPN = High: Write disable
17	DVDD	-	Digital Power Supply Input. Bypass DVDD to DGND with 10μF capacitor
18	OUT8	O	Gamma Reference Output
19	OUT9	O	Gamma Reference Output
20	OUT10	O	Gamma Reference Output
21	OUT11	O	Gamma Reference Output
22	OUT12	O	Gamma Reference Output
23	OUT13	O	Gamma Reference Output
24	OUT14	O	Gamma Reference Output
25	AGND	-	Ground of Analog Power Supply
26	RSET	O	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R_{SET}, from RSET to AGND to set the full-scale adjustable sink current
27	VI+	I	VCOM Amplifier Positive Input
28	VI-	I	VCOM Amplifier Negative Input

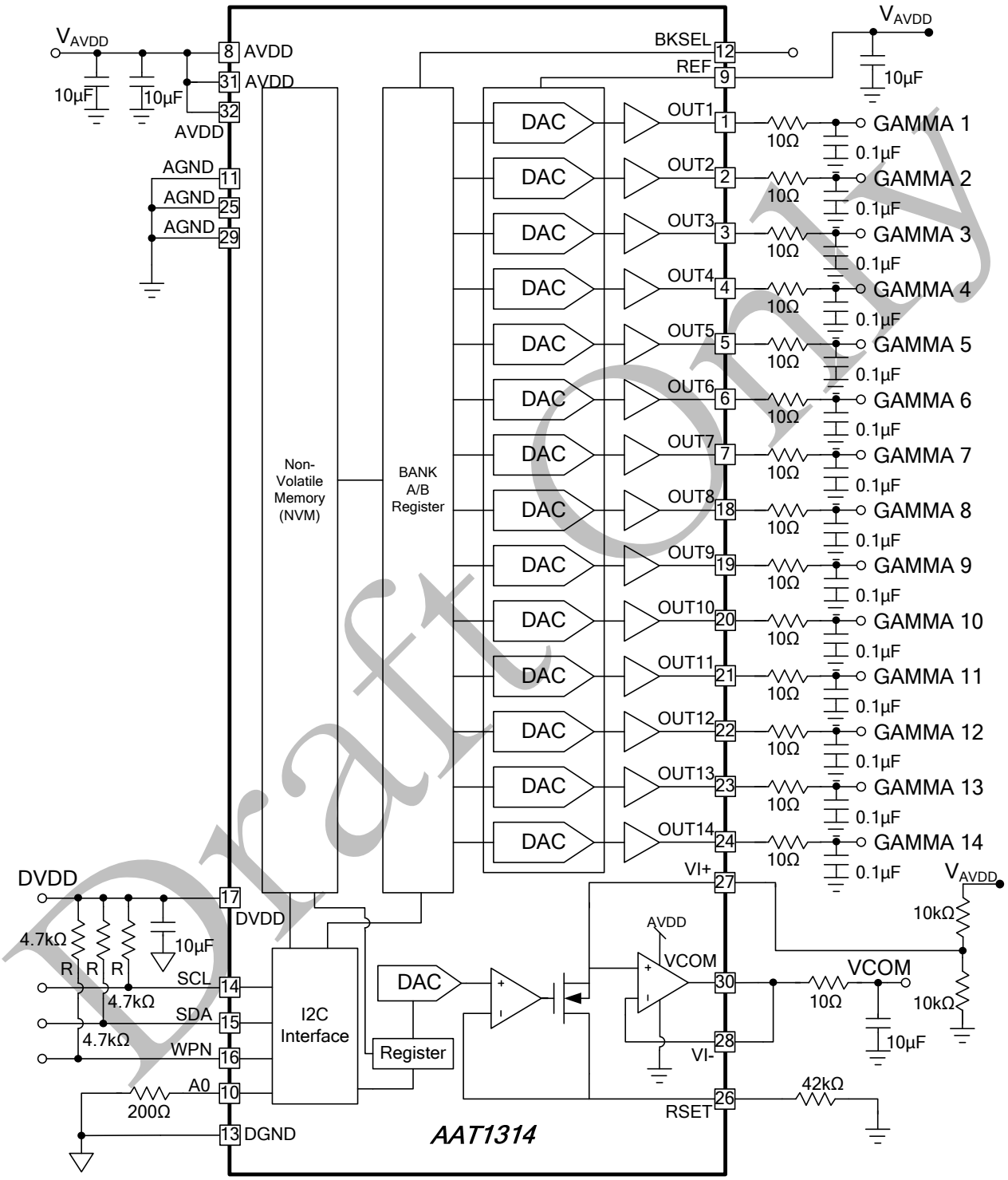
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
29	AGND	-	Ground of Analog Power Supply
30	VCOM	O	VCOM Amplifier Output
31	AVDD	-	Analog Power Supply Input. Bypass AVDD to AGND with 10µF capacitor
32	AVDD	-	Analog Power Supply Input. Bypass AVDD to AGND with 10µF capacitor

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



THEORY OF OPERATION

The AAT1314 integrates a programmable operational amplifier that drives the LCD backplane (VCOM), and also 14 channels of programmable gamma buffers for gamma collection. The device uses I^2C interface for setting such as output voltages, and for programming gamma and VCOM codes into multiple-time non-volatile memory (NVM).

Programmable GAMMA Buffers

The AAT1314 integrates 14 channel I^2C programmable gamma voltage generators to supply the source driver. The 14 channel gamma voltage generators also include non-volatile memory (NVM) to preserve the all programmed reference voltages by loading the nominal values from the NVM to the corresponding DAC when the device is powered. During device operation, each channel can be individually programmed by writing only to the corresponding DAC without transferring the programmed data to the NVM. In this case, the programmed voltages will not be retained when the device is powered down. Upon power up the DACs will be loaded with the default values that were already stored in the NVM. Note that the programmed DAC values can be transferred to the NVM via writing the appropriate command to the control register. When the DAC values are transferred to the NVM, the programmed gamma reference voltages will be preserved when the device is powered OFF, and retained when the device is powered back ON.

The output voltage of each channel is given by:

$$V_{OUTX} = \frac{N}{1023} \times VREF$$

Where N is the 10-bit digital word programmed to the gamma register, and VREF is the voltage at REF pin.

The PGAMMA reference generators are capable of generating voltages that are close to the upper and lower rails, AVDD and ground respectively. Note that the gamma reference generators are first passed to a gamma buffer to supply the source driver.

Programmable VCOM Operation Amplifier

The programmable VCOM operation amplifier can be used to digitally adjust a panel's VCOM voltage to remove flicker by controlling its output sink current. The programmable VCOM operation amplifier attaches to an external resistor-divider and sinks a programmable current I_{SET} to create the VCOM reference voltage. The external resistor R_{SET} sets the full-scale sink current and the minimum value of the VCOM reference voltage. The external resistor-divider and the AVDD supply set the maximum value of the VCOM reference voltage. The user can store the DAC setting in non-volatile memory. The resolution of the current DAC that generates I_{SET} is 7 bits (128 steps). Once the desired VCOM setting is obtained, the settings can be stored in the non-volatile memory, which would then be automatically recalled during every power-up. The DAC register and the non-volatile memory can be programmed through the I^2C interface. See the below figure.

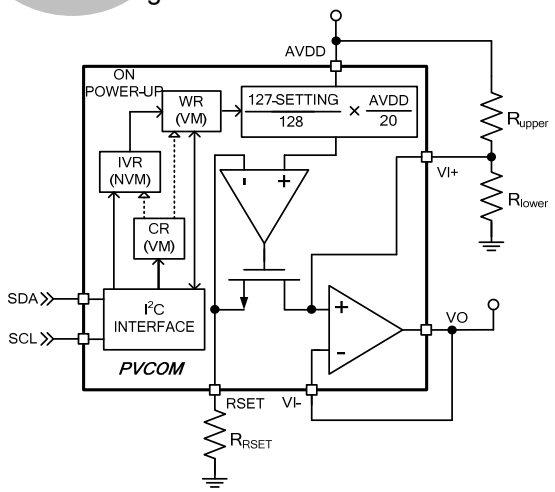


Figure 1. PVCOM Function Block of AAT1314.

The following equations determine the value of I_{SET}:

$$I_{SET} = \left(\frac{SETTING + 1}{128}\right) \times \left(\frac{V_{AVDD}}{20 \times R_{SET}}\right)$$

Where SETTING is the numeric value of the DAC's binary input code (0~127).

The programmable VCOM Operation Amplifier pulls I_{SET} through the external resistor divider comprised of

R_{UPPER} and R_{LOWER}. The resulting voltage V_{VCOM} is given by the following formula:

$$V_{VCOM} = \frac{R_{LOWER}}{R_{UPPER} + R_{LOWER}} \times V_{AVDD} \times \left(1 - \frac{SETTING + 1}{128} \times \frac{R_{UPPER}}{20 \times R_{SET}}\right)$$

During power up, the digital supply must be powered up first. The analog supply (AVDD) should not be powered up until the digital supply has stabilized. For power-down, analog supply must be powered down first to 0V, and then digital supply can safely be powered down.

Thermal Shutdown

The AAT1314 device enters into fault protection shutdown when the junction temperature reaches approximately 150°C. To restart the device when the junction temperature has fallen below the thermal shutdown threshold, recycle the device supply power below the UVLO falling threshold.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1314.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the DVDD and AVDD pin. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail.

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors and its load for best transient response.

Ground Plane

Use an analog ground plane for AGND pins. All analog ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create a digital ground plane (DGND) for DVDD bypass capacitor grounds. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (AGND) and digital ground (DGND) should be connected only at one signal point, near the expose pad by shorting the AGND pin to the expose pad.

I²C Protocol

When the R/W bit and A0 bit are 0 (such as in E8h), the master is indicating it will write data to the slave. If R/W = 1 and A0 is 0 (E9h in this case), the master is indicating it wants to read from the slave. During an I²C write operation, the master must transmit a register address to identify the memory location where the slave is to store the data. The register address is always the second byte transmitted during a write operation following the slave address byte.

During power-up, the values stored in the EE (EEPROM, non-volatile memory) are recalled into the DR (DAC Register, volatile memory).

The AAT1314 register addresses refer to the I2C interface register is shown below Table 1.

Table 1

Description	Symbol	Address		BIT 7	6	5	4	3	2	1	0	Default Value	BANK
OUT Enable	EN_{OUT}	00h	[1:1]	-		-			-	[1:1]	-	EN_{OUT} = 1	-
Write NVM	NVM_W		[3:3]	-		-		[3:3]	-		-	NVM_W = 0	
Read NVM	NVM_R		[4:4]	-		-	[4:4]		-		-	NVM_R = 0	
Temp. Enable	EN_{TEMP}		[6:6]	-	[6:6]	-			-		-	EN_{TEMP} = 0	
VCOM	M	01h	[7:1]	M[6]	M[5]	M[4]	M[3]	M[2]	M[1]	M[0]		CODE=64	
Gamma 1	G1	02h	[5:0]			G1[9]	G1[8]	G1[7]	G1[6]	G1[5]	G1[4]	CODE=512	A
		03h	[7:4]	G1[3]	G1[2]	G1[1]	G1[0]						
Gamma 2	G2	03h	[1:0]							G2[9]	G2[8]	CODE=512	A
		04h	[7:0]	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]		
Gamma 3	G3	05h	[5:0]			G3[9]	G3[8]	G3[7]	G3[6]	G3[5]	G3[4]	CODE=512	A
		06h	[7:4]	G3[3]	G3[2]	G3[1]	G3[0]						
Gamma 4	G4	06h	[1:0]							G4[9]	G4[8]	CODE=512	A
		07h	[7:0]	G4[7]	G4[6]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]		
Gamma 5	G5	08h	[5:0]			G5[9]	G5[8]	G5[7]	G5[6]	G5[5]	G5[4]	CODE=512	A
		09h	[7:4]	G5[3]	G5[2]	G5[1]	G5[0]						
Gamma 6	G6	09h	[1:0]							G6[9]	G6[8]	CODE=512	A
		0Ah	[7:0]	G6[7]	G6[6]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]		
Gamma 7	G7	0Bh	[5:0]			G7[9]	G7[8]	G7[7]	G7[6]	G7[5]	G7[4]	CODE=512	A
		0Ch	[7:4]	G7[3]	G7[2]	G7[1]	G7[0]						
Gamma 8	G8	0Ch	[1:0]							G8[9]	G8[8]	CODE=512	A
		0Dh	[7:0]	G8[7]	G8[6]	G8[5]	G8[4]	G8[3]	G8[2]	G8[1]	G8[0]		
Gamma 9	G9	0Eh	[5:0]			G9[9]	G9[8]	G9[7]	G9[6]	G9[5]	G9[4]	CODE=512	A
		0Fh	[7:4]	G9[3]	G9[2]	G9[1]	G9[0]						
Gamma 10	G10	0Fh	[1:0]							G10[9]	G10[8]	CODE=512	A
		10h	[7:0]	G10[7]	G10[6]	G10[5]	G10[4]	G10[3]	G10[2]	G10[1]	G10[0]		
Gamma 11	G11	11h	[5:0]			G11[9]	G11[8]	G11[7]	G11[6]	G11[5]	G11[4]	CODE=512	A

		12h	[7:4]	G11[3]	G11[2]	G11[1]	G11[0]						
Gamma 12	G12	12h	[1:0]							G12[9]	G12[8]	CODE=512	A
		13h	[7:0]	G12[7]	G12[6]	G12[5]	G12[4]	G12[3]	G12[2]	G12[1]	G12[0]		
Gamma 13	G13	14h	[5:0]			G13[9]	G13[8]	G13[7]	G13[6]	G13[5]	G13[4]	CODE=512	A
		15h	[7:4]	G13[3]	G13[2]	G13[1]	G13[0]						
Gamma 14	G14	15h	[1:0]							G14[9]	G14[8]	CODE=512	A
		16h	[7:0]	G14[7]	G14[6]	G14[5]	G14[4]	G14[3]	G14[2]	G14[1]	G14[0]		
Gamma 1	G1	25h	[5:0]			G1[9]	G1[8]	G1[7]	G1[6]	G1[5]	G1[4]	CODE=512	B
		26h	[7:4]	G1[3]	G1[2]	G1[1]	G1[0]						
Gamma 2	G2	26h	[1:0]							G2[9]	G2[8]	CODE=512	B
		27h	[7:0]	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]		
Gamma 3	G3	28h	[5:0]			G3[9]	G3[8]	G3[7]	G3[6]	G3[5]	G3[4]	CODE=512	B
		29h	[7:4]	G3[3]	G3[2]	G3[1]	G3[0]						
Gamma 4	G4	29h	[1:0]							G4[9]	G4[8]	CODE=512	B
		2Ah	[7:0]	G4[7]	G4[6]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]		
Gamma 5	G5	2Bh	[5:0]			G5[9]	G5[8]	G5[7]	G5[6]	G5[5]	G5[4]	CODE=512	B
		2Ch	[7:4]	G5[3]	G5[2]	G5[1]	G5[0]						
Gamma 6	G6	2Ch	[1:0]							G6[9]	G6[8]	CODE=512	B
		2Dh	[7:0]	G6[7]	G6[6]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]		
Gamma 7	G7	2Eh	[5:0]			G7[9]	G7[8]	G7[7]	G7[6]	G7[5]	G7[4]	CODE=512	B
		2Fh	[7:4]	G7[3]	G7[2]	G7[1]	G7[0]						
Gamma 8	G8	2Fh	[1:0]							G8[9]	G8[8]	CODE=512	B
		30h	[7:0]	G8[7]	G8[6]	G8[5]	G8[4]	G8[3]	G8[2]	G8[1]	G8[0]		
Gamma 9	G9	31h	[5:0]			G9[9]	G9[8]	G9[7]	G9[6]	G9[5]	G9[4]	CODE=512	B
		32h	[7:4]	G9[3]	G9[2]	G9[1]	G9[0]						
Gamma 10	G10	32h	[1:0]							G10[9]	G10[8]	CODE=512	B
		33h	[7:0]	G10[7]	G10[6]	G10[5]	G10[4]	G10[3]	G10[2]	G10[1]	G10[0]		
Gamma 11	G11	34h	[5:0]			G11[9]	G11[8]	G11[7]	G11[6]	G11[5]	G11[4]	CODE=512	B
		35h	[7:4]	G11[3]	G11[2]	G11[1]	G11[0]						
Gamma 12	G12	35h	[1:0]							G12[9]	G12[8]	CODE=512	B
		36h	[7:0]	G12[7]	G12[6]	G12[5]	G12[4]	G12[3]	G12[2]	G12[1]	G12[0]		
Gamma 13	G13	37h	[5:0]			G13[9]	G13[8]	G13[7]	G13[6]	G13[5]	G13[4]	CODE=512	B
		38h	[7:4]	G13[3]	G13[2]	G13[1]	G13[0]						
Gamma 14	G14	38h	[1:0]							G14[9]	G14[8]	CODE=512	B
		39h	[7:0]	G14[7]	G14[6]	G14[5]	G14[4]	G14[3]	G14[2]	G14[1]	G14[0]		

WRITE OPERATION

Write single byte to the DR (DAC Register):

Step 1: Master sends Start Condition.

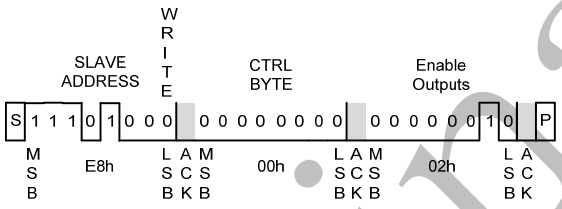
Step 2: Master sends the value E8h. (The AAT1314 address 1110100b and R/W bit = Low)
AAT1314 will acknowledge a bit for this byte.

Step 3: Send DR address (ex.00h, address of CTRL BYTE)
AAT1314 will acknowledge a bit for this byte

Step 4: Send the data to be written to the DR (ex.02h, enable outputs)
AAT1314 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Example: Writing 02h (enable outputs) to the DR address 00h (CTRL BYTE)



Write multiple bytes to the DR (DAC register):

Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (The AAT1314 address 1110100b and R/W bit = Low)
AAT1314 will acknowledge a bit for this byte.

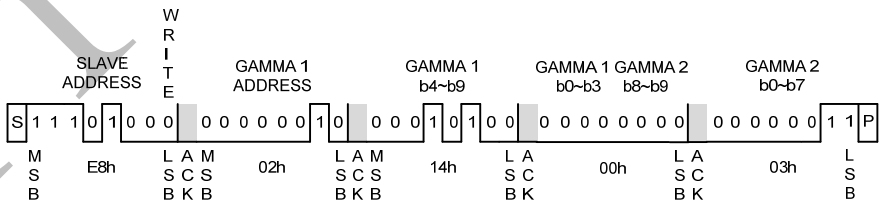
Step 3: Send DR address (ex.02h, address of GAMMA 1)
AAT1314 will acknowledge a bit for this byte

Step 4: Send the data to be written to the DR (ex.14h, GAMMA 1 b4~b9)
AAT1314 will acknowledge a bit for this byte

Step 5: Master continues sending the other bytes to be written to the DRs.
AAT1314 will acknowledge a bit for each byte and DR address will automatically increase

Step 6: Master sends Stop Condition.

Example: Writing 14h(GAMMA 1 b4~b9), 00h(GAMMA 1 b0~b3 & GAMMA 2 b8~b9), 03h(GAMMA 2 b0~b7) to the DR address 01h, 02h, 03h (GAMMA 1 & GAMMA 2)



Write all DR (DAC Register) data to EE (EEPROM):

Step 1: Master sends Start Condition.

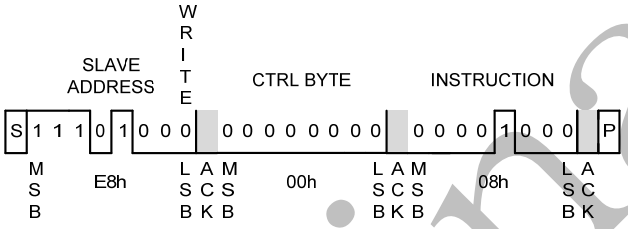
Step 2: Master sends the value E8h. (The AAT1314 address 1110100b and R/W bit = Low)
AAT1314 will acknowledge a bit for this byte.

Step 3: Send CTRL BYTE address (00h)
AAT1314 will acknowledge a bit for this byte

Step 4: Send the value 08h to make duplicate dates from DR to EE
AAT1314 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Example: Writing all DR data to EE at one time.



READ OPERATION

Read single data from DAC register (DR):

Step 1: Master sends the value E8h. (The AAT1314 address 1110100b and R/W bit = Low)
AAT1314 will acknowledge a bit for this byte.

Step 2: Send specified DR address to be read (ex.01h, address of PVCOM)
AAT1314 will acknowledge a bit for this byte

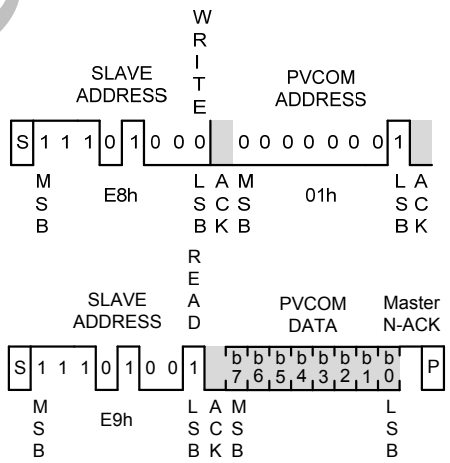
Step 3: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 4: Master sends the value E9h. (The AAT1314 address 1110100b and R/W bit = High)
AAT1314 will acknowledge a bit for this byte.

Step 5: Master read the data from DR and not-acknowledges for this byte.

Step 6: Master sends Stop Condition.

Example: Reading data from the DR addresses 01h (PVCOM)



Read multiple data from DAC register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (The AAT1314 PMIC address 1110100b and R/W bit = Low)
AAT1314 will acknowledge a bit for this byte.

Step 3: Send specified DR address to be read (ex.02h, address of GAMMA1)
AAT1314 will acknowledge a bit for this byte

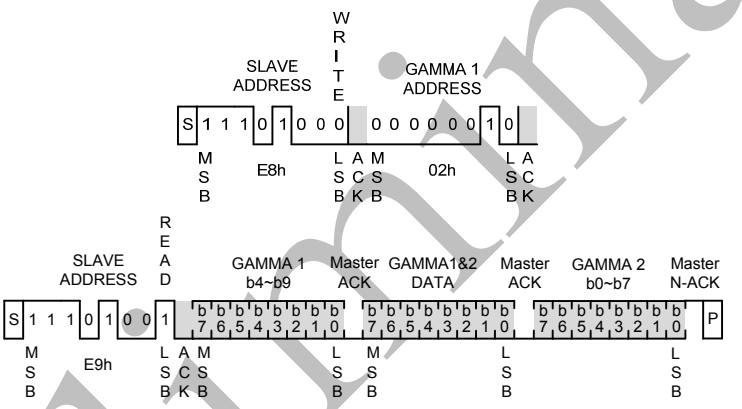
Step 4: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 5: Master sends the value E9h. (The AAT1314 address 1110100b and R/W bit = High)
AAT1314 will acknowledge a bit for this byte.

Step 6: Master continues read the data from DR and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The DR address will automatically increase

Step 7: Master sends Stop Condition.

Example: Reading data from the DR addresses 02h, 03h and 04h (GAMMA 1 & GAMMA 2)



Load all EE (EEPROM) data to DR (DAC Register):

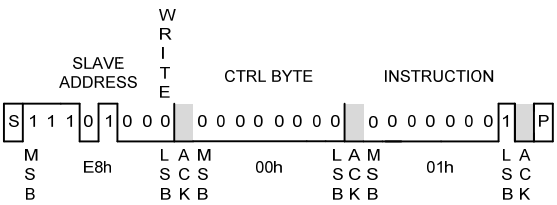
Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (The AAT1314 address 1110100b and R/W bit = Low)
AAT1314 will acknowledge a bit for this byte.

Step 3: Send CTRL BYTE address (00h)
AAT1314 will acknowledge a bit for this byte

Step 4: Send the value 01h to make duplicate dates from EE to DR
AAT1314 will acknowledge a bit for this byte

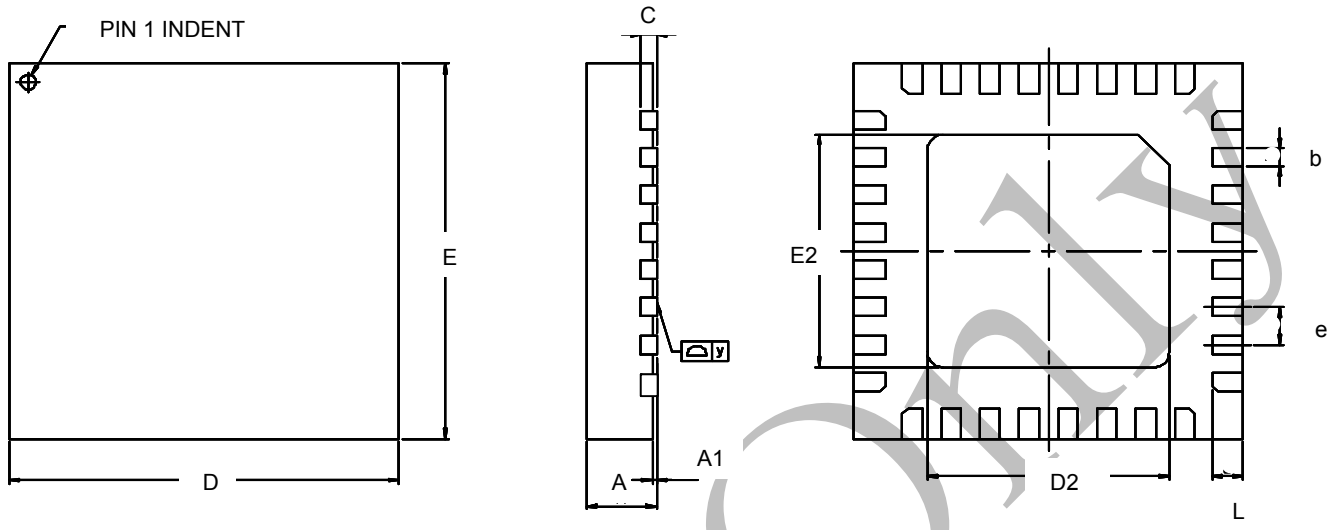
Step 5: Master sends Stop Condition.



S: Start Condition, P: Stop Condition, ☐: Master to Slave, ☐:Slave to Master

PACKAGE DIMENSION

WQFN32-5*5



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
C	------	0.2	------
D	4.9	5.0	5.1
D2	3.05	3.10	3.15
E	4.9	5.0	5.1
E2	3.05	3.10	3.15
e	------	0.5	------
L	0.35	0.40	0.45
y	0	------	0.075