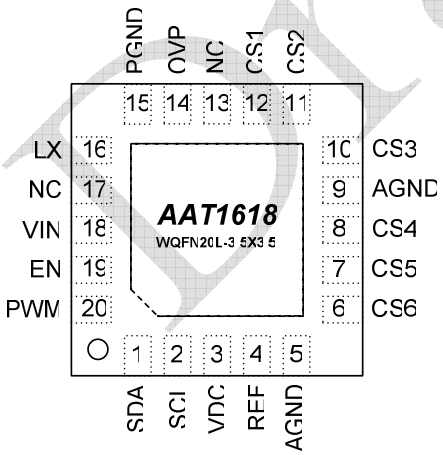
WHITE LEDS BACKLIGHT DRIVER

6-CHANNELS CURRENT BALANCING WITH PWM / MIX-MODE / DC DIMMING

FEATURES

- 2.5V to 24V Input Supply Voltage Range
- Fully I²C Interface Control
- Current Mode Boost Regulator for V_{LED}
  - Built-In 40V, 2.2A, 0.2Ω N-MOSFET
  - Internal Low-Dropout 5V Regulator
  - 450kHz~1.2MHz Programmable Switching Frequency
  - Built-in Soft-Start
- 6 Channel LED Current Sink Controller
  - Programmable LED Current Up to 30mA
  - Typical ±3% Current Accuracy
  - Typical ±2% Current Matching
  - PWM Dimming Frequency 100Hz~25KHz
  - PPM, PXM and PDM Dimming Control
- Protection
  - Over Voltage Protection (OVP)
  - WLED Open Protection
  - Over Temperature Protection (OTP)
- WQFN 20-3.5x3.5x0.75 Package Available

PIN CONFIGURATION



GENERAL DESCRIPTION

AAT1618 is a LED driver that consists of a Boost converter with a 6-channel current regulator. The device includes I²C interface for setting various parameters such as LED Sink current, switching frequency, dimming control, etc.

The device allows an input voltage range from 2.5V to 24V, thus suitable for applications in tablet and notebook backlight. The internal current mode Boost regulator provides the LED drive voltage. This Boost integrates a 40V, 0.2Ω power NMOS which allows the converter to drive up to 40V maximum. For system optimization, switching frequency can be programmed from 450KHz to 1.2MHz via I²C interface.

The device includes six identical LED current sink controllers that are adjustable up to 30mA with an accuracy of ±3% via I²C setting , and achieve a ±2% current mismatch between each channel.

The AAT1618 offers three kinds of dimming algorithm (PPM & PXM & PDM) for controlling the LED brightness via an external PWM dimming signal with an input frequency range of 100Hz to 25kHz. For PPM dimming the current sink controller is turn on/off, as determined by the PWM input signal. For PXM dimming, the current sink controller is a DC output current for input duty above 25%, and a PWM output current for input duty below 25%. For PDM dimming, the LED current is a DC current which is amplitude modulated by the PWM input. The benefits of PXM & PDM dimming include lower power consumption and minimal audible noise in the system. All of the dimming algorithms include jitter hysteresis and glitch cancellation for improved noised immunity.

The AAT1618 provides various protection mechanisms such as LED open protection, over-voltage protection, and thermal shutdown. The device is available in a small WQFN 20 pin 3.5mmx3.5mmx0.75mm with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40℃ to +85℃ temperature range.

APPLICATIONS

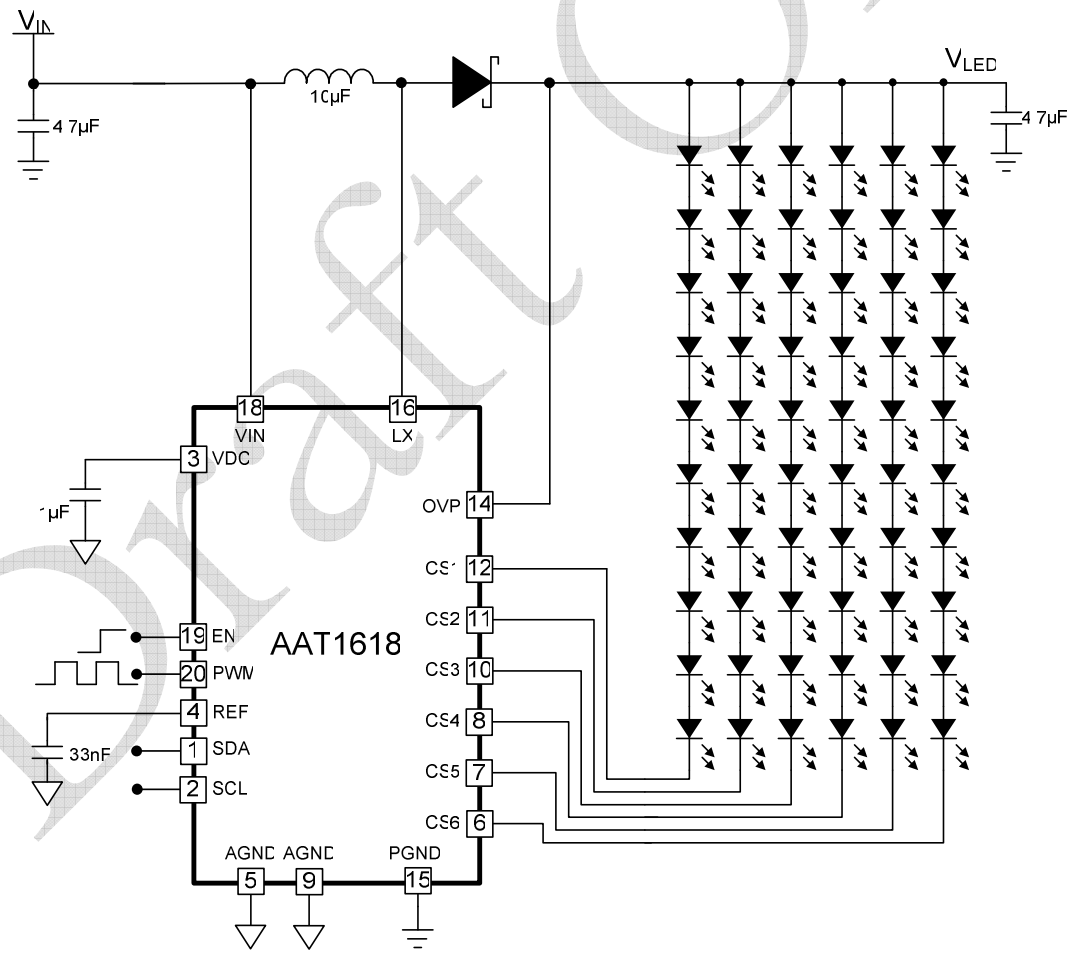
- Tablet LCD Panel Backlight
- Notebook LCD Panel Backlight

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMPRANGE	MARKING	MARKING DESCRIPTION
AAT1618	AAT1618-Q46-T	Q46: WQFN20L -3.5*3.5	T: Tape and Reel	−40°C to +85°C	AAT1618 XXXXXX XXXX	1. Part Name 2. Lot No. (6 Digits) 3. Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNIT
VOLTAGE RANGE	VIN, EN, PWM to AGND	V_{IN}	–0.3 to +30.0	V
	VDC, SDA, SCL, REF to AGND	V_{H1}	–0.3 to +6.0	V
	LX, CS1-CS6, OVP to PGND	V_{H2}	–0.3 to +40.0	V
	AGND to PGND	-	–0.3 to +0.3	V
HBM ESD RATING	VIN, EN, PWM, **SDA, SCL**, CS1-CS6 to GND	V_{HBM1}	8K	V
	All the other pins	V_{HBM2}	2K	V
MM ESD RATING	VIN, EN, PWM, **SDA, SCL**, CS1-CS6 to GND	V_{MM1}	400	V
	All the other pins	V_{MM2}	200	V
CDM ESD RATING		V_{CDM}	1K	V
Operating Ambient Temperature Range		T_A	–40 to +85	°C
Operating Junction Temperature Range		T_J	–40 to +150	°C
Storage Temperature Range		$T_{STORAGE}$	–65 to +150	°C
Package Thermal Resistance		θ_{JA}	TBD	°C /W
Power Dissipation, @ T_A = +25°C , T_J = +125 °C		P_d	TBD	W

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Supply Voltage	V_{IN}	2.5	24.0	V
LED Boost Output range	V_{LED}	V_{IN}+2V	39	V
Input PWM frequency	f_{PWM}	0.1	25	KHz
Minimum input PWM duty	D_{duty}	1	100	%
BOOST frequency	f_{OSC}	0.45	1.2	MHz
Operating Free-Air Temperature	T_A	–40	+85	°C

ELECTRICAL CHARACTERISTICS

(VIN=12V, EN =3.3V, f_{OSC} = 600kHz, I_{LED} = 20mA, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN Input Voltage Range	V_{IN}		2.5	-	24.0	V
VIN Under Voltage Lockout	V_{UVLO}	UVLO = 000	2	2.1	2.2	V
		UVLO = 001	2.3	2.5	2.7	V
		UVLO = 010	2.8	3.0	3.2	V
		UVLO = 011	3.3	3.5	3.7	V
		Others	3.8	4.0	4.2	V
		Hysteresis	100	200	300	mV
Quiescent Current	I_Q	V_{IN}=12V, EN=High LX no switching, PWM=0%	-	-	2	mA
Operating Current	I_{OS}	V_{IN}=12V, EN=High LX switching	-	5.0	-	mA
VDC Output Voltage	V_{LDO}	EN=High, V_{IN}>5.5V	4.8	5.0	5.2	V
VDC Output Current	I_{LDO}	V_{IN}=12V	-	50	70	mA
Shutdown Current	I_{SD}	V_{IN}=12V, EN=Low	-	-	10	µA
		V_{IN}=24V, EN=Low	-	-	15	µA
EN Input Low Voltage	V_{IL_EN}		**-**	**-**	**0.6**	V
EN Input High Voltage	V_{IH_EN}		**1.2**	**-**	**-**	V
EN Hysteresis of Trigger Input	V_{EN_HYS}		**0.15**	-	-	V
EN Input Pull Low Resistance	R_{EN}		300	-	1200	kΩ
Thermal Shutdown Temperature	T_{SD}	Rising Temperature	-	150	-	°C

ELECTRICAL CHARACTERISTICS

(VIN=12V, EN =3.3V, f_{OSC} = 600kHz, I_{LED} = 20mA, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Boost Regulator for VLED

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Maximum Output Voltage	V_{LED}		40	-	-	V
LX Oscillation Frequency	f_{OSC}	2 Bits, 450kHz/600kHz/ 800kHz/1200KHz	450	-	1,200	kHz
LX Oscillation Frequency Tolerance		Default Setting, 600kHz	–20	-	+20	%
LX Current Limit	I_{LIM_LX}	V_{IN}=12V	1.8	2.2	2.6	A
LX NMOS ON-Resistance	R_{ON_NMOS}	I_{LX}=1.0A	-	200	300	mΩ
LX Leakage Current	I_{Leak_NMOS}		-	-	20	µA
LX Maximum Duty Cycle	D_{MAX_LX}	V_{IN}=2.5V, V_{LED}=40V, η=80%, Maximum Rating	90	95	-	%
LX Minimum On Time	T_{MIN}		-	100	-	ns
Slew Rate during LX Switch OFF to ON Transient	**TS_{LX}**	**TS_{LX} = 00**		**2.2**		**V/ns**
		TS_{LX} = 01		**3.5**		**V/ns**
		TS_{LX} = 10		**4.8**		**V/ns**
		TS_{LX} = 11		**6**		**V/ns**
Slew Rate during LX Switch ON to OFF Transient	**TS_{LX}**	**TS_{LX} = 00**		**2.2**		**V/ns**
		TS_{LX} = 01		**3.5**		**V/ns**
		TS_{LX} = 10		**4.8**		**V/ns**
		TS_{LX} = 11		**6**		**V/ns**
Soft-Start Time	t_{SS}		-	10	-	ms
Delay Time	t_{DLY}		-	2	-	ms
OVP Threshold Voltage (OVP)	V_{OVP}	V_{LED} Rising	38	39	40	V
		V_{LED} Rising - V_{LED} Falling	-	0.5	-	V

ELECTRICAL CHARACTERISTICS

(VIN=12V, EN =3.3V, f_{OSC} = 600kHz, I_{LED} = 20mA, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Current Sink Controller

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
CSn Sink Current	I_{CS}	4 Bits, 1mA step	15	-	30	mA
Current Accuracy on Channels	I_{LEDA}	PPM (Duty : 1%~100%)	–3	-	+3	%
		PXM (Duty : 1%~100%)	–3	-	+3	%
		PDM (Duty : 15%~100%)	–3	-	+3	%
		PDM (Duty : 5%~15%)	–5	-	+5	%
		PDM (Duty : 1%~5%)	–8	-	+8	%
Current Mismatch on Channels	I_{LEDM}	PPM (Duty : 1%~100%)	–2	-	+2	%
		PXM (Duty : 1%~100%)	–2	-	+2	%
		PDM (Duty : 25%~100%)	–2	-	+2	%
		PDM (Duty : 5%~25%)	–2	-	+2	%
		PDM (Duty : 1%~5%)	–5	-	+5	%
Minimum CSn Regulation Voltage	V_{CS}	No LEDs Mismatch	-	500	600	mV
Maximum CSn Output Current	I_{CS_MAX}				30	mA
CSn Inrush current Percentage		Inrush(full-scale) / Full Scale			10	%
CSn Leakage Current					5	µA
DC Dimming Resolution		I_{CS}=15~25mA, PXM & PDM PWM Dimming=0.1~5kHz		1024		Steps
		I_{CS}=15~25mA, PXM & PDM PWM Dimming=5 ~10kHz		512		
		I_{CS}=15~25mA, PXM & PDM PWM Dimming=10 ~25kHz		256		
I_{CSn} Response Time		I_{CSn}=20mA, PXM & PDM PWM Duty 10%->90% @PWM Dimming=100Hz		20	25	ms
		I_{CSn}=20mA, PXM & PDM PWM Duty 10%->90% @PWM Dimming=25kHz		**80**	**100**	**µs**
OPEN Detection Voltage	V_{OPEN}		-	-	0.2	V

Note : 1. PPM : PWM to PWM Mode. 2. PXM : PWM to Mixed Mode. 3. PDM : PWM to DC Mode.

ELECTRICAL CHARACTERISTICS

(VIN=12V, EN =3.3V, f_{OSC} = 600kHz, I_{LED} = 20mA, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Dimming Control

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
PWM Input Frequency Range	f_{PWM}		100	-	25k	Hz
PWM Input Low Voltage	V_{IL_PWM}		**-**	**-**	**0.6**	**V**
PWM Input High Voltage	V_{IH_PWM}		**1.2**	**-**	**-**	**V**
PWM Hysteresis of Trigger Input	V_{PWM_HYS}		-	0.15	-	V
PWM Input Pull Low Resistance	R_{PWM}		300	-	1200	kΩ
PWM Minimum On Time					400	ns
PWM Deglitch Pulse Width		PWM Dimming: 100Hz~25kHz 11 bits data for hysteretic	110		125	ns
Mixed Mode Output Current Frequency		1% ≦ PWM Duty ≦25%	22.5	25.0	27.5	kHz

NVM

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Byte Write Time	t_{BYTE}		-	-	10	ms
Byte Read Access Time	B_{RT}		-	200	-	ns
NVM Programmable Times	N_{NVM}		-	1,000	-	Cycle

ELECTRICAL CHARACTERISTICS

(VIN=12V, EN =3.3V, f_{OSC} = 600kHz, I_{LED} = 20mA, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

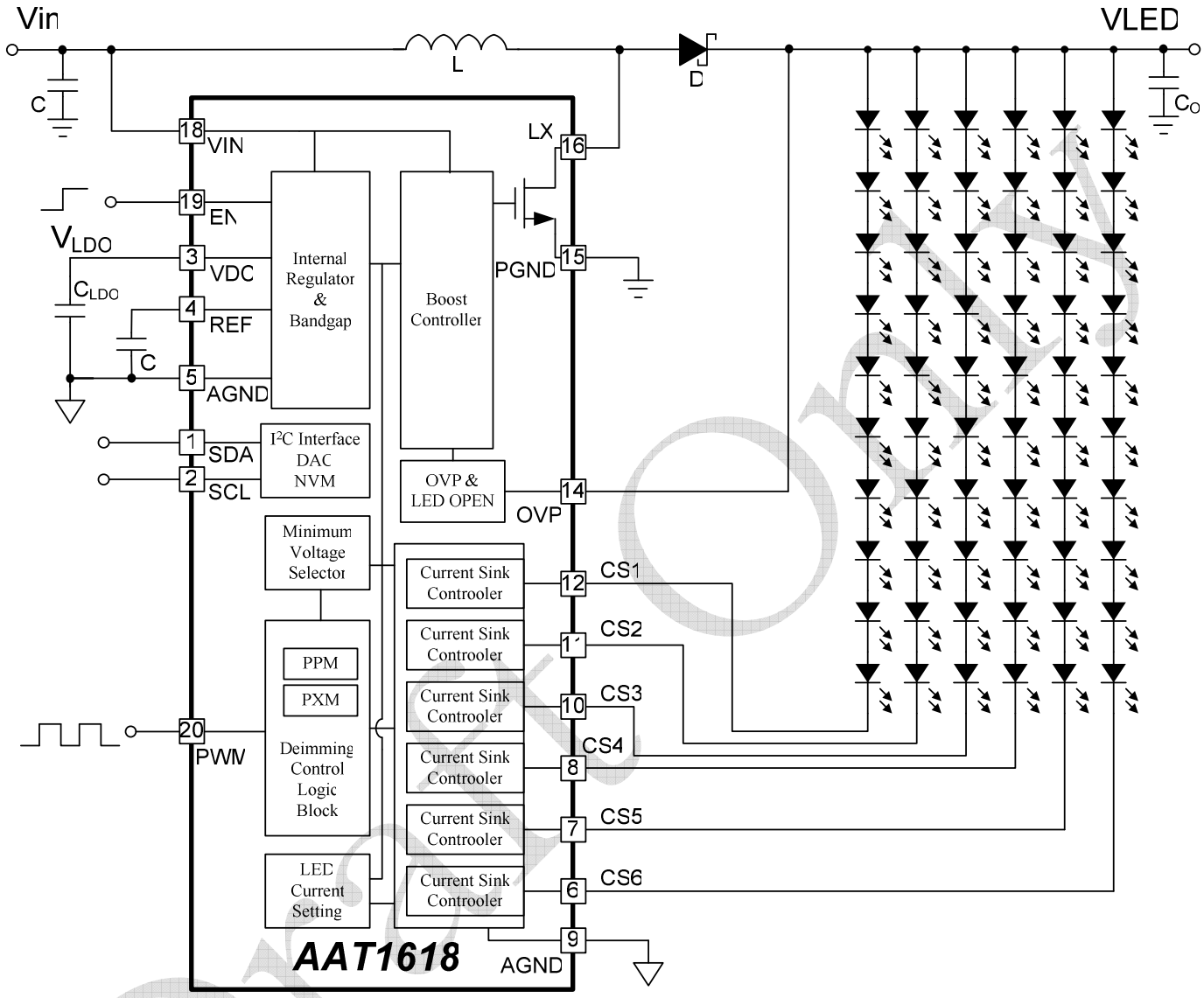
I²C Interface

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCL, SDA Input High Voltage	V_{IH2}		1.2	-	-	V
SCL, SDA Input Low Voltage	V_{IL2}		-	-	0.6	V
SCL, SDA Input Capacitance	C_{SI}		-	5p	-	F
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA	-	-	0.4	V
SCL Clock Frequency	f_{OSCI2C}		-	-	400k	Hz
SCL Clock High Period	t_{IH3}		0.6	-	-	µs
SCL Clock Low Period	t_{IL3}		1.3	-	-	µs
SCL, SDA Receiving Rise Time	t_{R1}		-	20+0.1* C_B	300	ns
SCL, SDA Receiving Fall Time	t_{F1}		-	20+0.1* C_B	300	ns
I²C Data Setup Time	t_{S1}		100	-	-	ns
I²C Data Hold Time	t_{H1}		-	-	900	ns
I²C Setup Time for START Condition	t_{S2}		0.6	-	-	µs
I²C Hold Time for START Condition	t_{H2}		0.6	-	-	µs
I²C Bus Free Time Between STOP and START Conditions	t_{BUS}		4.7	-	-	µs
I²C Pulse Width of Suppressed Spike	t_{PS}		-	-	50	ns
I²C Bus Capacitance	C_B		-	-	400	pF
SDA, SCL Pull Up resistor	R_{PU}		4.7	10.0	-	kΩ

PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	SDA	I	I^2C Compatible Serial Data Input/Output
2	SCL	I	I^2C Compatible Serial Clock Input
3	VDC	O	Internal LDO output and supply rail for the logic power
4	REF	O	The Reference Pin for Internal Error Amplifier.
5	AGND	-	Analog Ground
6	CS6	I	Current Sink Controller Pin
7	CS5	I	Current Sink Controller Pin
8	CS4	I	Current Sink Controller Pin
9	AGND	-	Analog Ground
10	CS3	I	Current Sink Controller Pin
11	CS2	I	Current Sink Controller Pin
12	CS1	I	Current Sink Controller Pin
13	NC	-	No Connection
14	OVP	I	Over Voltage Protection Setting Input
15	PGND	-	Power Ground
16	LX	O	Switch Node of LED Boost Regulator
17	NC	-	No Connection
18	VIN	I	Power Supply Input
19	EN	I	Enable Pin
20	PWM	I	PWM Dimming Control Pin

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

The AAT1618 consists of a Boost converter, an internal regulator, six channel current sink controller with balancing, and PPM (PWM to PWM Mode) & PXM (PWM to MIX-Mode) & PDM (PWM to DC Mode) dimming control logic for applications in LCD panel backlight.

Shutdown Control (EN)

The AAT1618 can be disabled to reduce the supply current to 15µA when EN pin is pulled low, and can be powered up when EN pin is at high level. Note that when the EN pin is left floating, the AAT1618 is still disabled via an internal pull-low resistor.

Under Voltage Lockout (UVLO)

For systematic startup, AAT1618 employs a UVLO threshold which can be programmed for either 2.1V, 2.5V, 3.0V, 3.5V, or 4V. Thus, the input supply must exceed the UVLO threshold for the regulators to begin startup. Likewise, the device shuts down all functions when the input voltage is lower than hysteresis threshold of 200mV. The hysteresis voltage is added to prevent device chattering when the input supply is noisy or unstable during power up or power down.

Internal Regulator (VDC)

The AAT1618 includes an internal LDO which serves to accept a high voltage input supply. The LDO supplies a low voltage to the internal circuitry of the boost, LED current sink controller and digital control logic. A 1µF output capacitor of low ESR/ESL is recommended and should be placed as close to the VDC pin as possible.

Thermal Shutdown (OTP)

The AAT1618 device enters into fault protection shutdown when the junction temperature reaches approximately 150°C. To restart the device when the junction temperature has fallen below the thermal shutdown threshold, recycle the device supply power or EN below the UVLO falling threshold.

Boost Regulator for V_{LED}

The boost regulator uses a peak current mode control scheme that integrated low R_{DSON} (typical 0.2Ω) NMOS, built-in 2ms soft start to provides fast output response during transients, and also simple compensation.

The LX switching frequency can be programmed for either 450kHz, 600kHz, 800kHz, or 1.2MHz and the LX switching ON/OFF transient slew rate can be set from 0.5V/ns to 1.1V/ns with 0.2V/ns steps via I^2C interface. This boost regulator is a compact and economical solution but also provides design in flexibility. The boost regulator operates from a minimum input voltage of 2.5V, and delivers an output voltage that reaches the maximum capable duty cycle. The duty cycle (D) is calculated by

$$D = \frac{V_O - V_I}{V_O} \quad \text{or} \quad \frac{V_O}{V_I} = \frac{1}{1-D}, \quad (V_O = V_{LED})$$

where V_O (V_{LED}) is the output of the boost regulator.

At the heart of the current mode topology are two feedback loops. See the AAT1618 Boost Regulator Functional Block Diagram Figure 1.

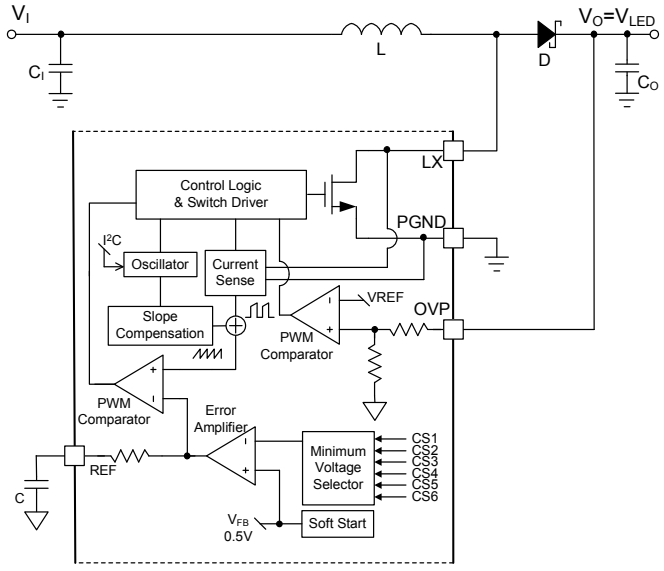


Figure 1. Boost Regulator Functional Block Diagram

One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal power switch. The second loop monitors the voltage via minimum voltage selector between LED current sink controller CS1 to CS6 and compares the minimum voltage to an internal reference voltage of 0.5V using a transconductance error amp. Regulation is achieved by modulating the internal power switch ON time. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles above 50%. During each rising edge of the internal clock pulse, the power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

Boost Current Limit

When the Boost NMOS switch current exceeds 2.2A, the current limit function disables the gate driver of this boost regulator and prevents the internal NMOS from switching. Once switch current falls below the 2.2A threshold, the boost will resume switching. The current limit value is clamped to a lower value at power-on and will reach the final value of 2.2A after soft-start.

Internal Soft Start

AAT1618 employs a soft-start feature to limit the inrush current. The internal soft-start circuit prevents the excessive inrush current, input voltage drop and output voltage overshoot. The soft-start timing chart is shown below.

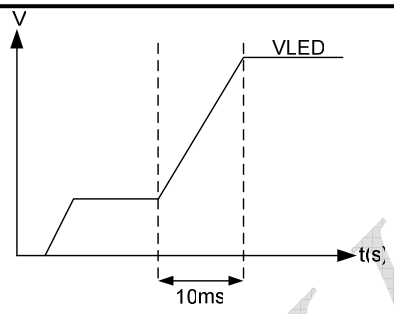


Figure 2. Soft-Start Timing Chart

Over Voltage Protection (OVP) for AVDD

The AAT1618 offers a over-voltage protection to prevent over-voltage damage to the IC and other components. When the boost output exceeds its Over Voltage Protection threshold (typ. 39V), the AAT1618 disables the gate driver of this boost regulator and prevents the internal NMOS from switching. Once output voltage falls below the OVP threshold, with a hysteresis of approximately 0.5V, the boost will resume switching.

LED Current Sink Controller

The AAT1618 includes six identical LED current sink controllers that can be set from 15mA to 30mA with 1mA steps via I^2C interface, and offers three kinds of dimming algorithm (PPM & PXM & PDM) for controlling the LED brightness. For any unused LED channel, it is recommended to connect the respective unused CSn pin to ground.

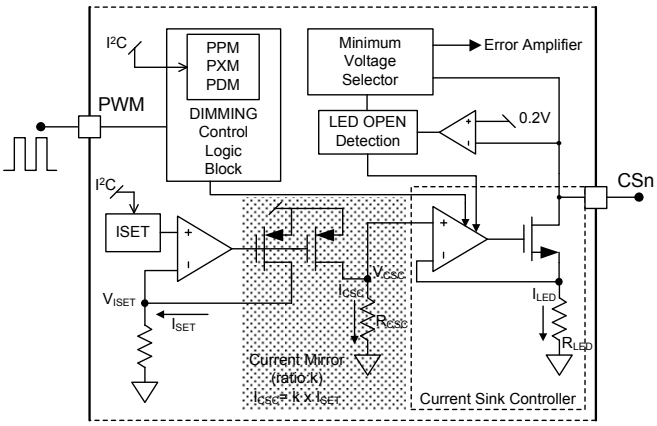


Figure 3. Current Sink Control Functional Block Diagram

DIMMING Control (Mode Selection)

The AAT1618 offers three kinds of dimming control and can be select through the MODE register via I^2C interface. See below Table 1 for the register Table of Dimming MODE Setting.

MODE Register	Dimming Cotrol	Note
00	PPM : PWM to PWM Mode	
01	PXM : PWM to Mix-1 Mode	
10	PDM : PWM to DC Mode	
11	PXM : PWM to Mix-2 Mode	25kHz

Table 1

The benefits of PXM & PDM dimming include lowers overall power consumption, eliminates audible noise in systems, prevents excessive inrush currents for the Boost converter, eliminates Boost output ripple, and minimizes system EMI. Note that the AAT1618 PWM input includes jitter hysteresis and glitch cancellation for improved noised immunity.

PPM (PWM to PWM MODE)

For PPM dimming, a PWM signal is applied to the PWM pin. The LED current is synchronized with PWM input logic signal and there is no phase delay between each current sink. The LED Current frequency is equivalent to PWM input frequency. See Figure 4 for reference.

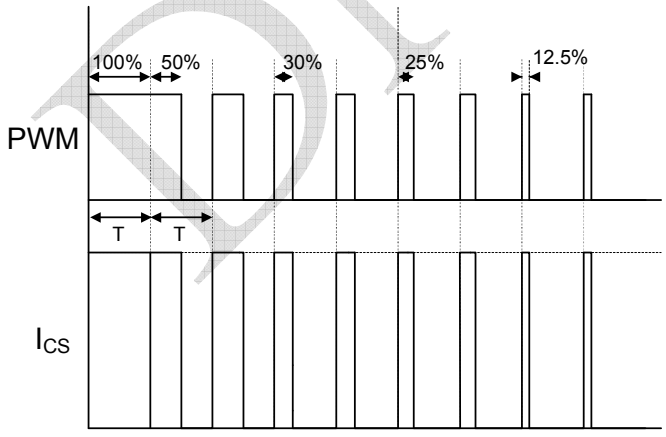


Figure 4. PPM Dimming Timing Chart

PXM (PWM to MIX-MODE)

For PXM dimming, the device is in PWM to MIX-Mode (Figure 5). In this mode, the PWM signal to I_{CS} dimming cycle is delayed by 2 periods. The first cycle delay is for the duty counter. The second cycle delay is for duty rate calculation.

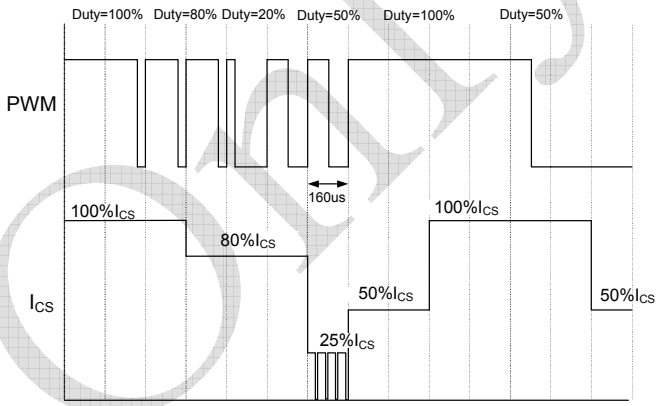


Figure 5. PXM Dimming Timing Chart

PXM dimming consists of both DC and PWM LED output current depending on the duty cycle:

(a) When 25%≦PWM input duty≦100%, the LED output current is DC and the PWM duty cycle modulates the amplitude of the current. See Figure 5.

(b) Below 25% input duty cycle, the DC LED output current will translate to PWM to control the LED current. For this PWM output current, the LED current amplitude is fixed at 0.25 x I_{CS} and the dimming duty will be at 4 x PWM input duty. If PWM to Mix-1 Mode was setting, the dimming frequency is the same as PWM input, and if dimming frequency is fixed around 22.5kHz to 27.5kHz, it is in PWM to Mix-2 Mode.

Note that if EN input is low during PXM MODE (Figure 6), the duty counter and duty calculation does not operate. If EN input is high, the duty counter and duty calculation will initiate two complete periods before it turns on the LED.

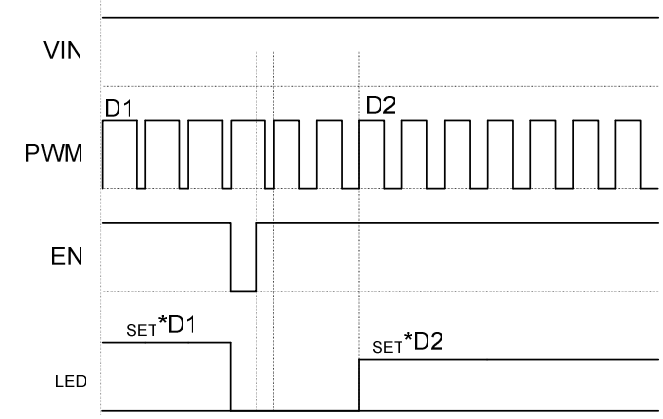


Figure 6. LED Current Control Using PXM Dimming Mode (EN on/off Control)

PDM (PWM to DC MODE)

For PDM dimming, the AAT1618 accepts a PWM input signal which modulates the amplitude of the DC current that drives the CSn. See Figure 7 for reference.

Note that the I_{CS} Dimming cycle is delayed by 2 periods from the PWM signal. The first cycle delay is for the duty counter. The second cycle is for calculating the duty rate. The six channels sink DC current and the PWM duty cycle modulates the amplitude of the DC current.

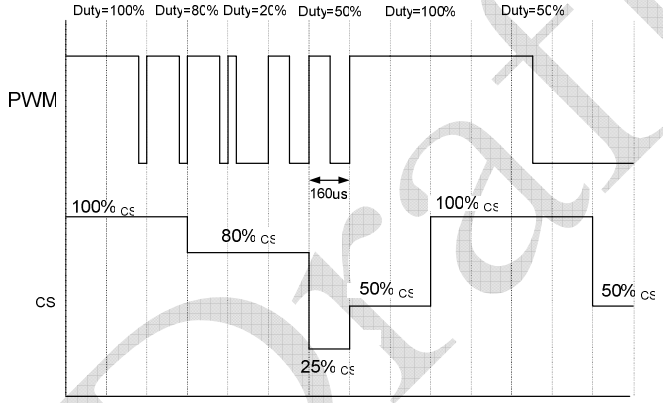


Figure 4. PDM Dimming Timing Chart

LED Open-Circuit Protection

When one or more CS strings are open, the CSn voltage of the open channel will be pulled low and the COMP pin will be driven high. The boost converter duty cycle and the output voltage will increase. Once the boost output voltage rises high enough to reach the OVP threshold, and simultaneously the CSn voltage drops below the CS Open Detection Voltage of 0.2V, the open CS channels will turn off. If the open CS channels recover and rise above the CS Open Detection Voltage of 0.2V, the open CS channels will turn on again.

I²C Serial Interface

The AAT1618 features an I²C-compatible, 2-wire serial interface consisting of a SDA and a SCL. SDA and SCL are an I/O with an open-drain output that requires a pull up resistor to realize high-logic levels. Pull up resistor values should be chosen to ensure that the rise and fall times are within specification. A typical value for the pull up resistors is 4.7kΩ. Each slave on the I²C bus responds to a slave address byte sent immediately following a Start Condition. Below diagram shows the definition of timing on I²C bus:

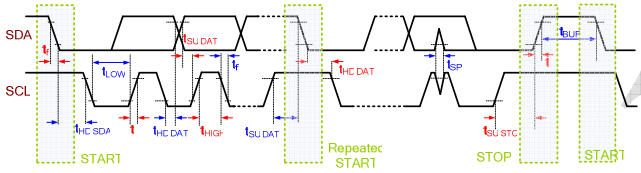


Figure 13. Definition of timing on I²C bus

The slave address byte contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit. Below diagram shows the slave addresses:

Table 3. Slave Address byte

1	0	1	1	0	0	0	R/$\overline{W}$

MSB LSB

I²C Protocol

When the R/W bit is 0 (such as in B0h), the master is indicating it will write data to the slave. If R/W = 1 (B1h in this case), the master is indicating it wants to read from the slave. During an I2C write operation, the master must transmit a register address to identify the memory location where the slave is to store the data. The register address is always the second byte transmitted during a write operation following the slave address byte. The AAT1618 PMIC register addresses refer to the I2C register map.

During power-up, the values stored in the EE (EEPROM, nonvolatile memory) are recalled into the DR (DAC Register, volatile memory).

WRITE OPERATION

Write Single Byte To DR (DAC Register):

Step 1: Master sends Start Condition.

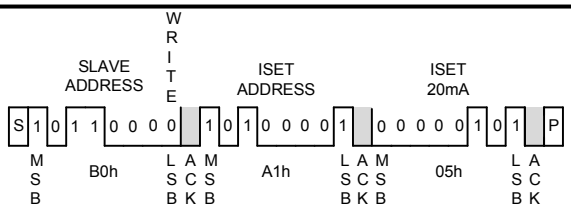
Step 2: Master sends the value B0h. (the AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

Step 3: Send DR address (ex.A1h, address of ISET)
AAT1618 will acknowledge a bit for this byte.

Step 4: Send the data to be written to the DR (ex.05h, ISET = 20mA) AAT1618 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Example: Writing 05h (20mA) to the DR address A1h (ISET)



Write Multiple Bytes To DR (DAC Register):

Step 1: Master sends Start Condition.

Step 2: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

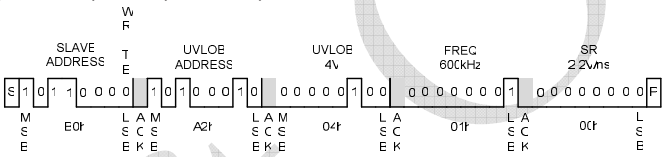
Step 3: Send DR address (ex.A2h, address of UVLOB)
AAT1618 will acknowledge a bit for this byte.

Step 4: Send the data to be written to the DR (ex.04h, UVLOB=4V) AAT1618 will acknowledge a bit for this byte.

Step 5: Master continues sending the other bytes to be written to the DRs. AAT1618 will acknowledge a bit for each byte and DR address will automatically increase.

Step 6: Master sends Stop Condition.

Example: Writing 04h(4V), 01h(600kHz), 00h(2.2V/ns) to the DR address A2h, A3h, A4h (UVLOB, FREQ, SR)



Write All DR (DAC Register) Data To EE (EEPROM):

Step 1: Master sends Start Condition.

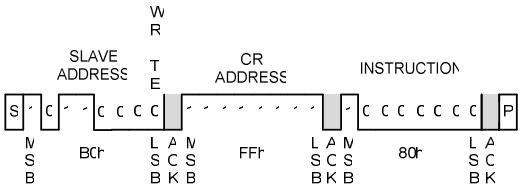
Step 2: Master sends the value B0h. (the AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

Step 3: Send CR (Control Register) address (FFh)
AAT1618 will acknowledge a bit for this byte.

Step 4: Send the instruction 10000000b (X: Don't care, ex. 80h) to make duplicate data from DR to EE. AAT1618 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Example: Writing all DR data to EE.



READ OPERATION

Read Single Data From DAC Register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value B0h. (the AAT1618 PMIC address 1011000b and R/W bit = Low)

AAT1618 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1618 will acknowledge a bit for this byte.

Step 4: Send the instruction 00000000b (X: Don't care, ex. 00h) to specify that the data is read from the DR. AAT1618 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.05h, address of AVDD) AAT1618 will acknowledge a bit for this byte.

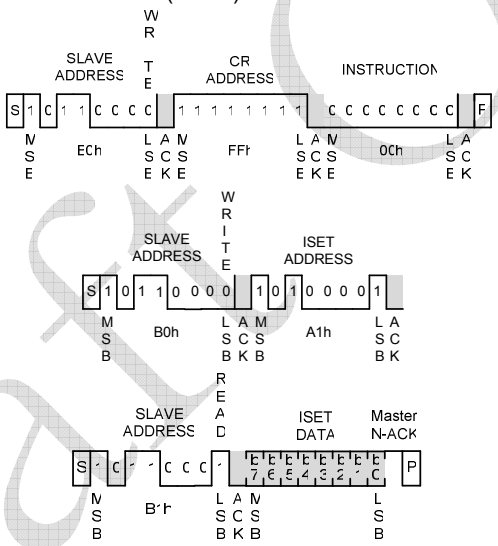
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value B1h. (the AAT1618 PMIC address 1011000b and R/W bit = High)
AAT1618 will acknowledge a bit for this byte.

Step 11: Master read the data from DR and not-acknowledges for this byte.

Step 12: Master sends Stop Condition.

Example: Reading data from the DR addresses A1h (ISET)



Read Multiple Data From DAC Register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1618 will acknowledge a bit for this byte.

Step 4: Send the instruction 0XXXXXX0b (X: Don't care, ex. 00h) to specify that the data is read from the DR. AAT1618 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low)

AAT1618 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.A2h, address of UVLOB) AAT1618 will acknowledge a bit for this byte.

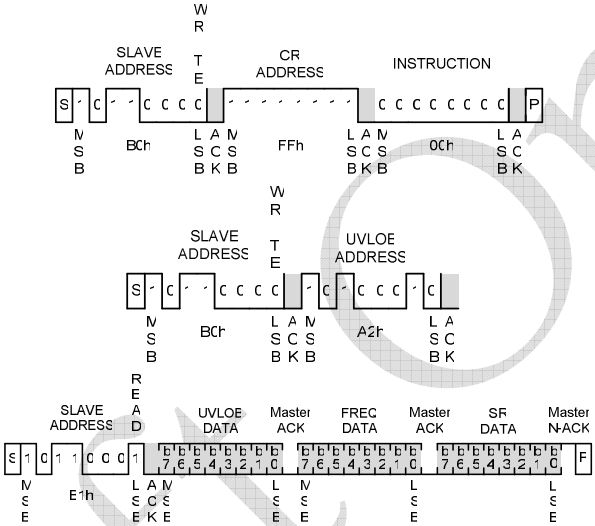
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value B1h. (The AAT1618 PMIC address 1011000b and R/W bit = High)
AAT1618 will acknowledge a bit for this byte.

Step 11: Master continues read the data from DR and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The DR address will automatically increase.

Step 12: Master sends Stop Condition.

Example: Reading data from the DR addresses A2h, A3h, A4h (UVLOB, FREQ, SR)



Read Single Data From EEPROM (EE):

Step 1: Master sends Start Condition.

Step 2: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1618 will acknowledge a bit for this byte.

Step 4: Send the instruction 0XXXXXX1b (X: Don't care, ex. 01h) to specify that the data is read from the EE. AAT1618 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

Step 8: Send specified EE address to be read (ex.A1h, address of ISET) AAT1618 will acknowledge a bit for this byte.

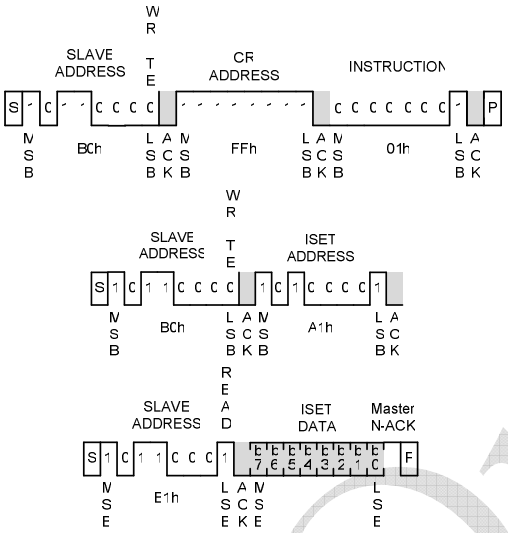
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value B1h. (The AAT1618 PMIC address 1011000b and R/W bit = High)
AAT1618 will acknowledge a bit for this byte.

Step 11: Master read the data from EE and not-acknowledges for this byte.

Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses A1h (ISET)



Read Multiple Data From EEPROM (EE):

Step 1: Master sends Start Condition.

Step 2: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low) AAT1618 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1618 will acknowledge a bit for this byte

Step 4: Send the instruction 0XXXXXX1b (X: Don't care, ex. 01h) to specify that the data is read from the EE. AAT1618 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value B0h. (The AAT1618 PMIC address 1011000b and R/W bit = Low)
AAT1618 will acknowledge a bit for this byte.

Step 8: Send specified EE address to be read (ex.A2h, address of UVLOB) AAT1618 will acknowledge a bit for this byte.

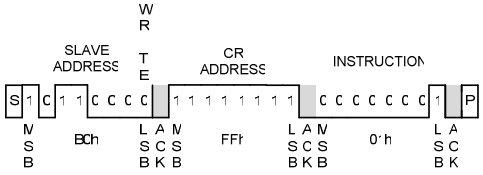
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

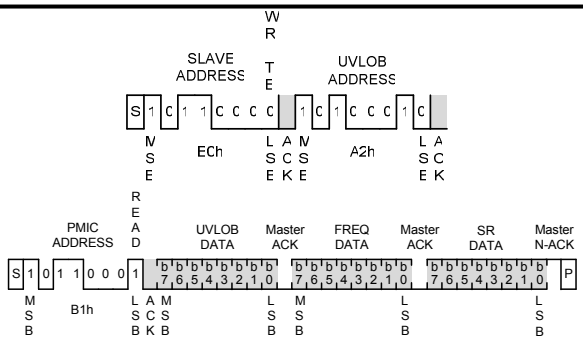
Step 10: Master sends the value B1h. (The AAT1618 PMIC address 1011000b and R/W bit = High)
AAT1618 will acknowledge a bit for this byte.

Step 11: Master continues read the data from EE and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The EE address will automatically increase.

Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses A2h, A3h, A4h (UVLOB, FREQ, SR)





S: Start Condition, P: Stop Condition, X: Don't Care.

: Master to Slave, :Slave to Master

LED I2C INTERFACE REGISTER DESCRIPTION

REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
A0h	MODE	02h	Sets brightness dimming mode
A1h	ISET	05h	Sets the current sinks full scale current
A2h	UVLO	03h	Sets the input voltage UVLO threshold
A3h	FREQ	01h	Sets the boost switching frequency
A4h	SR	00h	Sets the boost switching slew rate
A5h	CONFIG	00h	Sets the error amplifier compensation
A6h	Others	00h	Sets the compensation method and thermal shutdown flow
FFh	Control	00h	Controls whether read and write operations access RAM or EEPROM registers

LED DAC REGISTER SETTING DESCRIPTION

MODE (00h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						MODE	

00	PPM : PWM to PWM Mode
01	PXM : PWM to Mix-1 Mode
10	PDM : PWM to DC Mode
11	PXM : PWM to Mix-2 Mode

ISET (A1h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				ISET			

0000	I_{CS} = 15 mA	1000	I_{CS} = 23 mA
0001	I_{CS} = 16 mA	1001	I_{CS} = 24 mA
0010	I_{CS} = 17 mA	1010	I_{CS} = 25 mA
0011	I_{CS} = 18 mA	1011	I_{CS} = 26 mA
0100	I_{CS} = 19 mA	1100	I_{CS} = 27 mA
0101	I_{CS} = 20 mA	1101	I_{CS} = 28 mA
0110	I_{CS} = 21 mA	1110	I_{CS} = 29 mA
0111	I_{CS} = 22 mA	1111	I_{CS} = 30 mA

UVLO (A2h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					UVLO		

000	V_{UVLO} = 2.0 V
001	V_{UVLO} = 2.5 V
010	V_{UVLO} = 3.0 V
011	V_{UVLO} = 3.5 V
101	V_{UVLO} = 4.0 V
Others	V_{UVLO} = 4.0 V

FREQ (A3h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						FREQ	

00	f_{OSC} = 450 kHz
01	f_{OSC} = 600 kHz
10	f_{OSC} = 800 kHz
11	f_{OSC} = 1200 kHz

TSLX (A4h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						TS_{LX}	

00	Tf = 2.2 V/ns Tr = 2.2 V/ns
01	Tf = 3.5 V/ns Tr = 3.5 V/ns
10	Tf = 4.8 V/ns Tr = 4.8 V/ns
11	Tf = 6.0 V/ns Tr = 6.0 V/ns

CONFIG (A5h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					COMP		OCP_T

OCP_T	Bits	This bit enable/disable the OCP fault protect time 2ms	
	[0]	0	Disable the OCP 2ms Shutdown
		1	Enable the OCP 2ms Shutdown
COMP	Bits	These bits configure the current compensation current control for LED Boost Regulator	
	[2:1]	00	Typ.
		01	TBD
		10	TBD
		11	TBD

Others (A6h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						Temp	Comp

Comp	Bits	This bit selects the compensation method of boost converter	
	0	0	External compensation by connecting the capacitor from REF pin to GND
		1	Internal compensation
Temp	Bits	This bit selects the control flow of thermal shutdown	
	0	0	Latch
		1	Non-latch and with 40°C hysteresis

CONTROL (FFh)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
WED	Reserved						RED

RED	Bits	The state of this bit determines whether read operations return the contents of the DAC registers or the contents of the EEPROM	
	0	0	Read operations return the contents of the DAC registers
		1	Read operations return the contents of the EEPROM
VGHT	Bits	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned	
	6:1		
VGL	Bits	Setting this bit forces the contents of all DAC registers to be copied into EEPROM, thereby making them the default values during power-up When the contents of all the DAC registers have been written to the EEPROM, the AAT1618 automatically resets this bit.	
	7		

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1618.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VIN and VDC pins. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VIN and VDC bypass capacitor should refer to analog ground (AGND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost regulator contains the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node LX. The input bulk capacitance should also be placed close to these power path components to shorten the power ground length between the input and output.

Feedback and Compensation Components

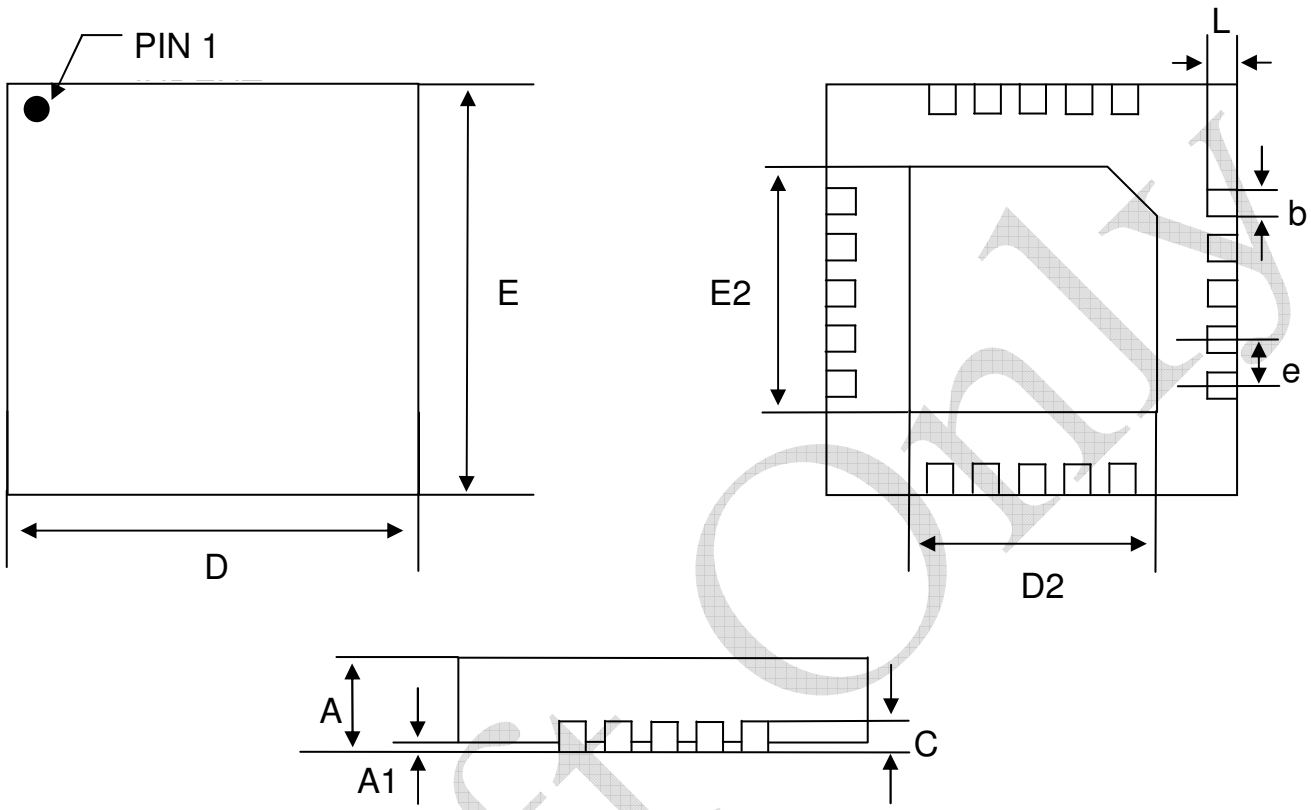
Any components for feedback, such as the resistive divider networks for setting the output voltage, should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise pickup. Likewise, compensation components should be placed as close as possible to the pin or device.

Ground Plane

Use a power ground plane for the boost output capacitor ground, for the boost input bulk capacitor ground, and PGND pin. All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create an analog ground plane for VIN and VDC pins, bypass capacitor grounds, compensation component ground, feedback resistive network grounds, and also the AGND pin. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (AGND) and power ground (PGND) should be connected only at one signal point, near the expose pad by shorting the AGND pins to the expose pad.

PACKAGE DIMENSION

WQFN20L-3.5mmX3.5mmX0.9mm



Symbol	Dimensions In Millimeters		
	Min	TYP	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.18	0.25	0.3
C	-----	0.2	-----
D	-----	3.5	-----
D2	1.9	2	2.1
E	-----	3.5	-----
E2	1.9	2	2.1
e	-----	0.5	-----
L	0.35	0.4	0.45