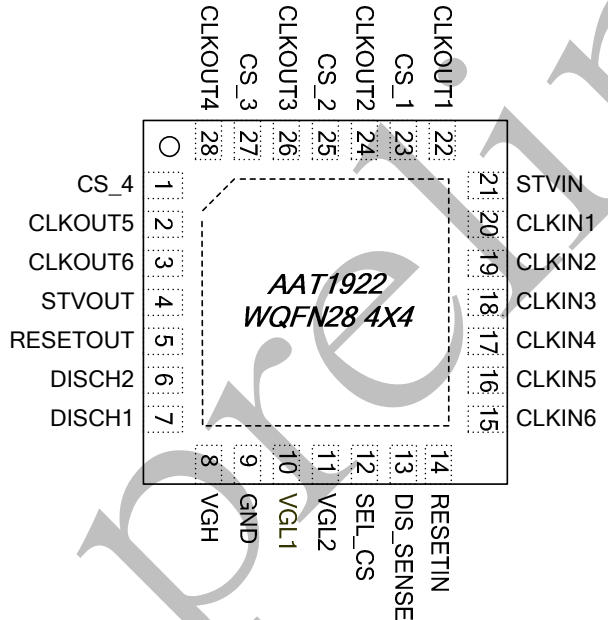
LEVEL SHIFTER FOR TFT LCD GOA PANEL

8-CHANNEL LEVEL SHIFTER WITH CHARGE-SHARING AND PANEL DISCHARGE

FEATURES

- **STVOUT Output for STVIN**
- **RESETOUT Output for RESETIN**
- **6-Channel CLKOUTx Outputs for CLKINx**
  - **Charge-Sharing Selectable**
- **DISCH1 & DISCH2 Outputs for Panel Discharge**
- **Level-Shifter Supply Voltage Range**
  - **Max. +45V for High Level (VGH)**
  - **Min. –20V for Low Level (VGL1 & VGL2)**
- **Protection**
  - **Under-Voltage Lockout (UVLO)**
  - **Over Temperature Protection (OTP)**
- **WQFN28-4x4 Package Available**

PIN CONFIGURATION



GENERAL DESCRIPTION

The AAT1922 contains 8 channel level-shifter scan drivers which are designed to drive the TFT panels with row drivers integrated on the panel glass. Each level-shifter can swing from +42V to –18V and features low impedance output stages that achieve fast rise and fall times even when driving the capacitive loading typically present in LCD display applications.

The scan-driver outputs (STVOUT, RESETOUT, and CLKOUT1~CLKOUT6) converts the logic-level signals generated by the Timing Controller (T-CON) to the high-level signals used by the display panel. And the clock outputs (CLKOUTx) support normal operation and two different charge-sharing methods for improving TFT LCD image quality and power consumption.

DISCH1 and DISCH2 driver outputs are the dedicated discharge channel. It works with the integrated voltage detector. When system power down, the voltage detector will command the discharge channel DISCH1 and DISCH2 to swing its output to VGH so as to remove residual image quickly.

The AAT1922 provides various protection mechanisms such as input under-voltage lockout (UVLO) and over temperature protection. The device is available in a small WQFN 28 pin 4x4x0.75mm with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40°C to +85°C temperature range.

APPLICATIONS

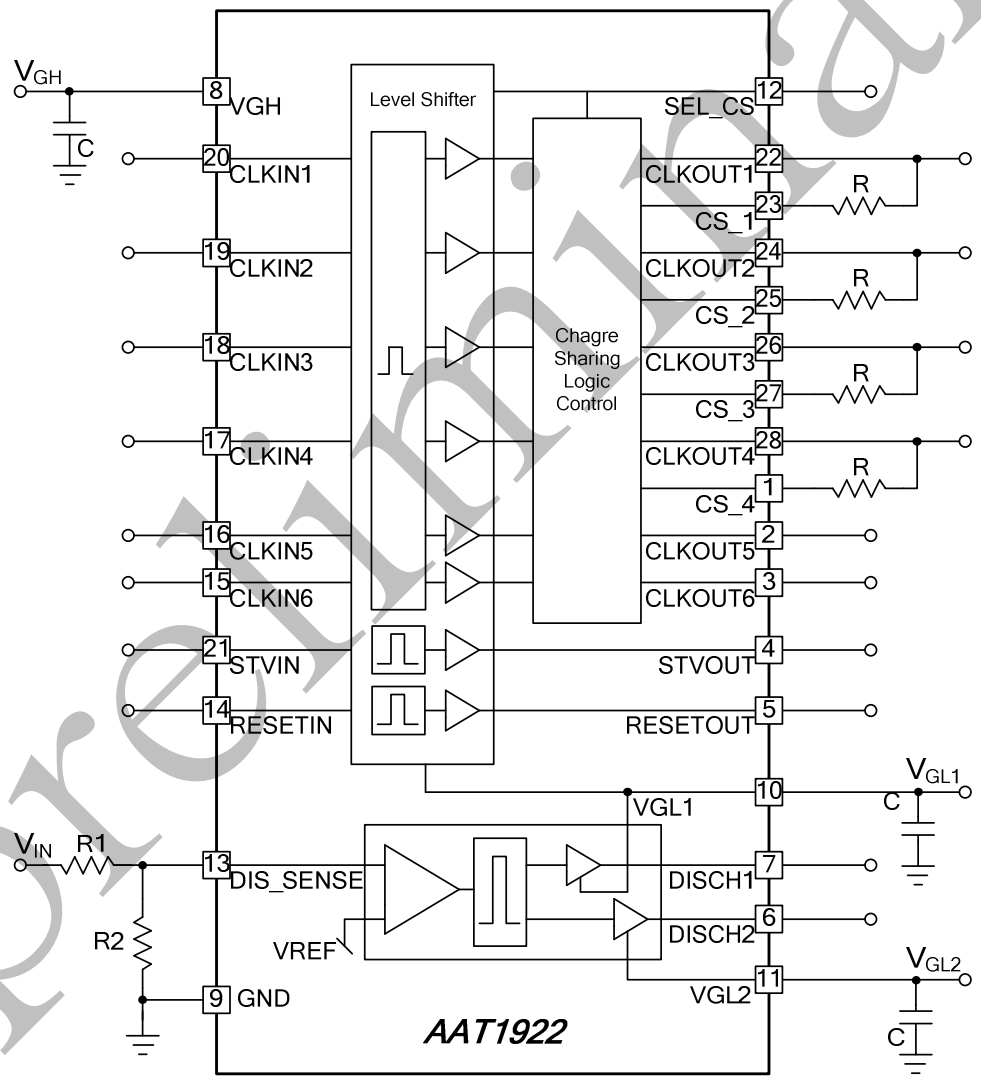
- **TFT LCD GOA Panel**

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1922	AAT1922-Q44-T	Q44:WQFN 28-4x4	T: Tape and Reel	−40°C to +85°C	1922 XXXXX XXXX	Device Type Lot no. (4~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VGH to GND	V_{GH}	–0.3 to +50	V
VGL1 to GND	V_{GL1}	–20 to +0.3	V
VGL2	V_{GL2}	$–0.3+V_{GL1}$ to 0.3	V
VGH to VGL1, VGH to VGL2	V_G	60	V
Input Voltage (STVIN, CLKIN1, CLKIN2, CLKIN3, CLKIN4, CLKIN5, CLKIN6, RESETIN, DIS_SENSE, SEL_CS)	V_I	–0.3 to +6.0	V
Output Voltage (STVOUT, CLKOUT1, CLKOUT2, CLKOUT3, CLKOUT4, CLKOUT5, CLKOUT6, CS_1, CS_2, CS_3, CS_4, RESETOUT, DISCH1)	V_O	$–0.3+V_{GL1}$ to $V_{GH}+0.3$	V
DISCH2	V_O	$–0.3+V_{GL2}$ to $V_{GH}+0.3$	V
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Range	θ_{JA}	28.5	°C / W
Power Dissipation @ T_A = +25°C , T_J = +125°C	P_d	3.51	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
VGH Input Voltage Range	V_{GH}	16.5	42.0	V
VGL1, VGL2 Input Voltage Range	V_{GL}	–18	–3	V
Voltage Difference Between V_{GH} and V_{GLx}	V_G	-	60	V

ELECTRICAL CHARACTERISTICS

(V_{GH} = 30V, V_{GL1} = –10V, V_{GL2} = –8V T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VGH Input Voltage Range	V_{GH}	VGH–VGL < 60V	16.5	-	45.0	V
VGL1 Input Voltage Range	V_{GL1}	VGH–VGL < 60V	–18	-	–3	V
VGL2 Input Voltage Range	V_{GL2}	VGH–VGL < 60V	–18	-	–3	V
Operating Frequency	f_{OSC}		-		500	kHz
V_{GH}–V_{GLX} Voltage Range	V_{GH}–V_{GLX}		-	-	60	V
VGH Supply Current	I_{Q_VGH}		-	-	850	uA
VGH Under Voltage Lockout Threshold	V_{GH_UVLO}	Rising	13.5	15.0	16.5	V
		Falling	2.0	3.5	5.0	V
Thermal Shutdown	T_{SHDN}		130	150	170	°C

Input Signals (STVIN, CLKINx, RESETIN, DIS_SENSE, SEL_CS)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Low level Input Voltage	V_{IL}		-	-	0.8	V
High level Input Voltage	V_{IH}		2	-	-	V
Charge-Sharing Threshold Voltage	V_{SEL_CS}	Disable	0	-	0.5	V
		Enable, Mode 1	1	-	2	
		Enable, Mode 2	2.8	-	6.5	
SEL_CS Internal Pull-Low Resistor	R_{SEC_CS}		50	100	150	kΩ
Input Current (SEL_CS)		SEL_CS = 5V	-	50	100	μA
Level Shifter Input Pull Low Resistance	R_{IN}		50	100	200	kΩ
Discharge Threshold Voltage	V_{REF}		1.14	1.20	1.26	V

ELECTRICAL CHARACTERISTICS

(V_{GH} = 30V, V_{GL1} = –10V, V_{GL2} = –8V T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature)

Level Shifter Outputs (CLKOUTx, CS_x)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
STVOUT1&2, VGPOUT1&2, CLKOUTx Rising Propagation Delay Time	T_{RPD}	C_{OUT} = 150pF	-	40	100	ns
STVOUT1&2, VGPOUT1&2, CLKOUTx Falling Propagation Delay Time	T_{FPD}	C_{OUT} = 150pF	-	50	100	ns
CLKOUTx Rising Charge Sharing Propagation Delay Time	t_{RPD_CS}	C_{OUT} = 150pF, R_{CS} = 50Ω	-	50	150	ns
CLKOUTx Falling Charge Sharing Propagation Delay Time	t_{FPD_CS}	C_{OUT} = 150pF, R_{CS} = 50Ω	-	70	150	ns
Slew Rate	SR+	C_{OUT} = 4.7nF, V_{OUT} = 20% to 80%	50	140	-	V/µs
	SR-		50	150	-	V/µs
Internal Charge-Sharing Resistance	R_{CS}	I_{CS} = 10mA	30	60	100	Ω
High-Side Switch-On Resistance	r_{DSON_H1}	I_{OUT} = 10mA, sourcing (High Side)	-	11	25	Ω
Low-Side Switch-On Resistance	r_{DSON_L1}	I_{OUT} = –10mA, Sinking (Low Side)	-	7	15	Ω

Level Shifter Outputs (STVOUT, RESETOUT)

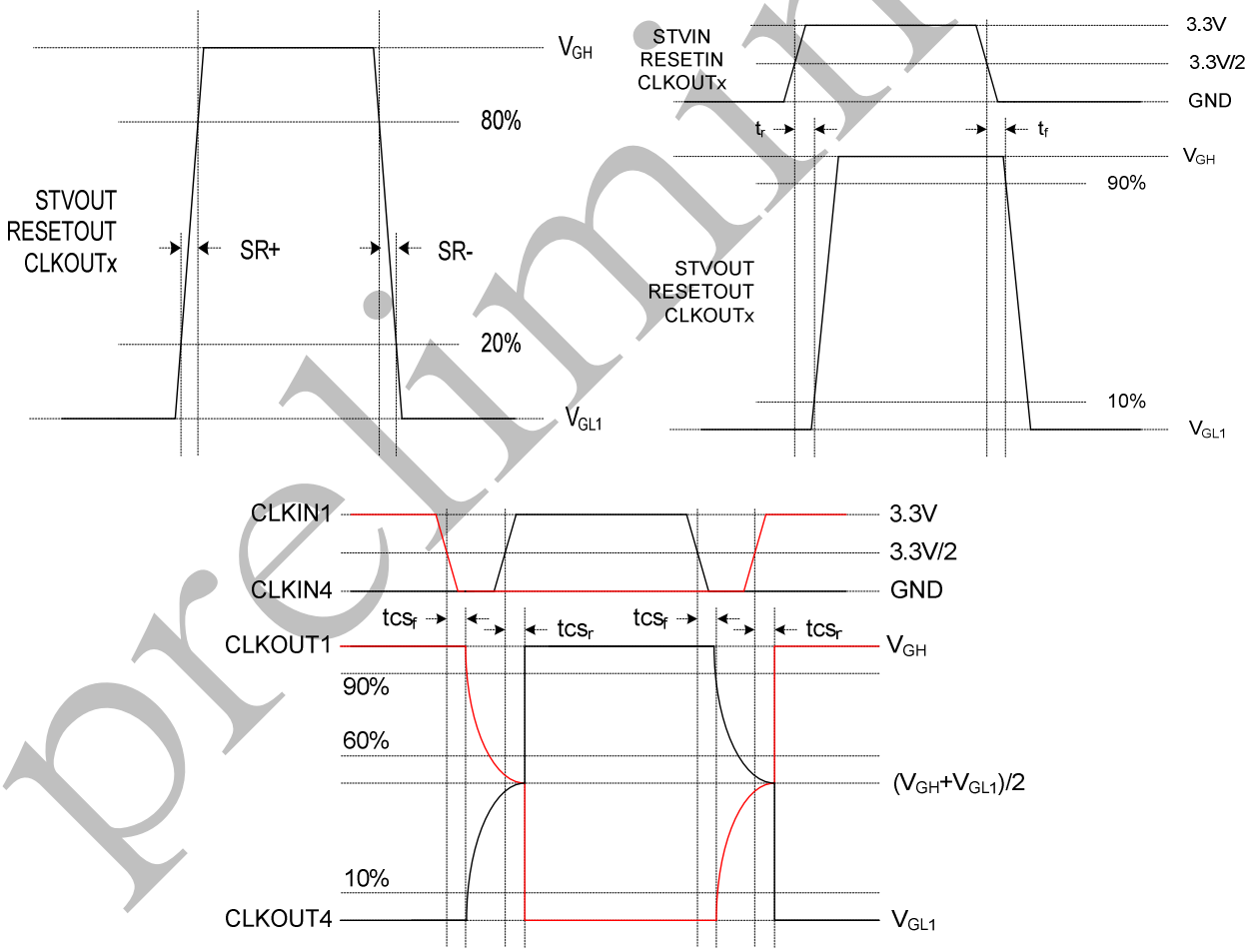
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Rising Propagation Delay Time	t_{RP2}	C_{OUT} = 150pF	-	40	100	ns
Falling Propagation Delay Time	t_{FP2}	C_{OUT} = 150pF	-	50	100	ns
Slew Rate	SR+	C_{OUT} = 4.7nF, V_{OUT} = 20% to 80%	20	50	-	V/µs
	SR–		30	60	-	V/µs
High-Side Switch-On Resistance	r_{DSON_H2}	I_{OUT} = 10mA, sourcing (High Side)	-	30	60	Ω
Low-Side Switch-On Resistance	r_{DSON_L2}	I_{OUT} = –10mA, Sinking (Low Side)	-	15	30	Ω

ELECTRICAL CHARACTERISTICS

(V_{GH} = 30V, V_{GL1} = –10V, V_{GL2} = –8V T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature)

Level Shifter Outputs (DISCH1, DISCH2)

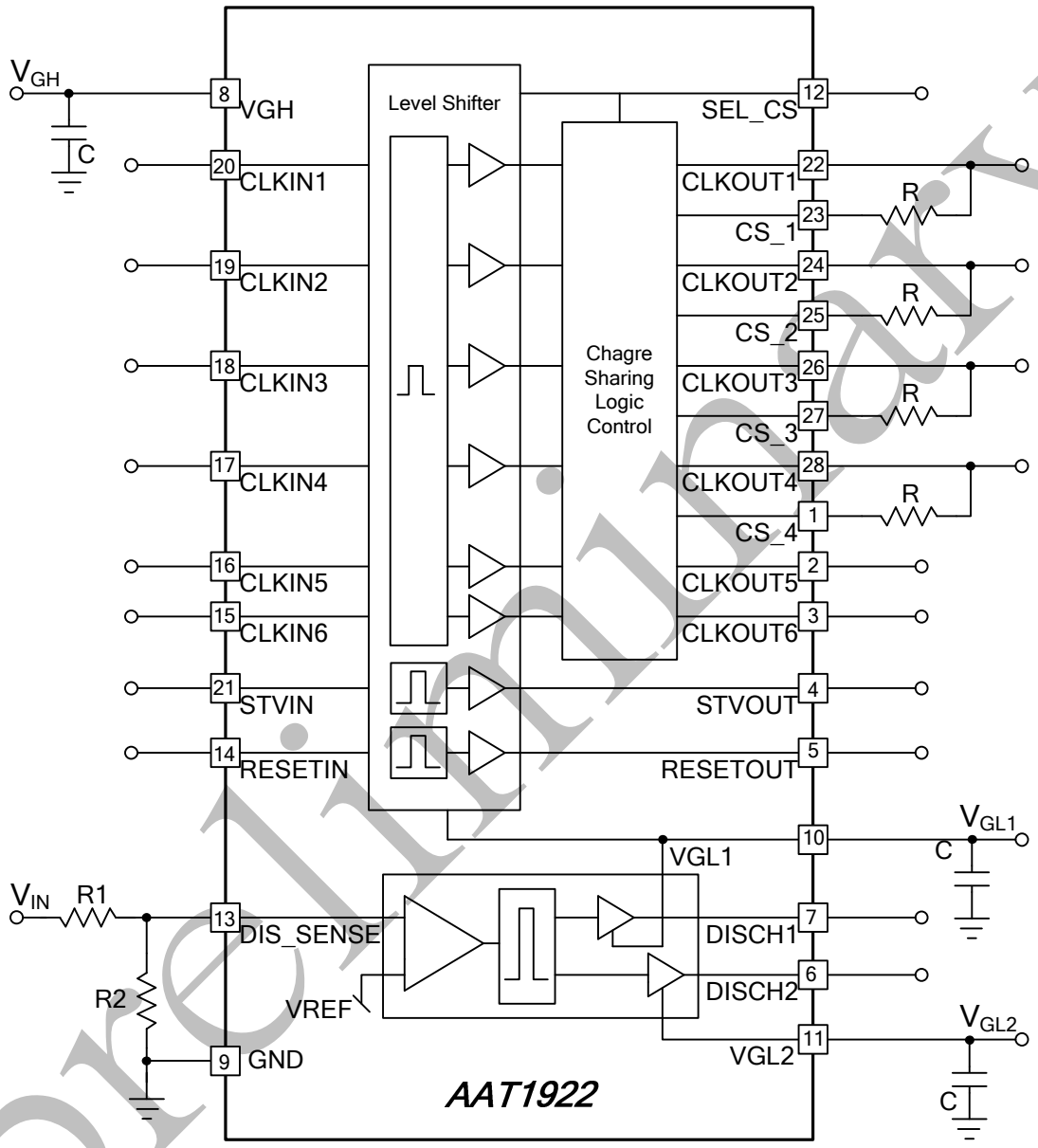
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
DISCH1 High-Side Switch-On Resistance	r_{DSON_H3}	I_{OUT} = 10mA, Sourcing (High Side)	-	14	60	Ω
DISCH1 Low-Side Switch-On Resistance	r_{DSON_L3}	I_{OUT} = –10mA, Sinking (Low Side)	-	10	20	Ω
DISCH2 High-Side Switch-On Resistance	r_{DSON_H4}	I_{OUT} = 10mA, Sourcing (High Side)	-	14	60	Ω
DISCH2 Low-Side Switch-On Resistance	r_{DSON_L4}	I_{OUT} = –10mA, Sinking (Low Side)	-	10	20	Ω



PIN DESCRIPTION

PIN NO	NAME	I/O	DESCRIPTION
1	CS_4	I/O	Clock 4 Charge-Sharing Input
2	CLKOUT5	I/O	Level Shift Clock 5 Output
3	CLKOUT6	I/O	Level Shift Clock 6 Output
4	STVOUT	O	Level Shift STV Output
5	RESETOUT	O	Level Shift RESET Output
6	DISCH2	O	Level Shift Discharge Output 2
7	DISCH1	O	Level Shift Discharge Output 1
8	VGH	P	Positive Supply Voltage
9	GND	-	Ground
10	VGL1	P	Negative Supply Voltage for All Outputs except DISCH2 Output
11	VGL2	P	Negative Supply Voltage for DISCH2 Output
12	SEL_CS	I	Charge-Sharing Mode Selection Terminal.
13	DIS_SENSE	I	Voltage Sense Input for Discharge Function
14	RESETIN	I	Level Shift RESET Input
15	CLKIN6	I	Level Shift Clock 6 Input
16	CLKIN5	I	Level Shift Clock 5 Input
17	CLKIN4	I	Level Shift Clock 4 Input
18	CLKIN3	I	Level Shift Clock 3 Input
19	CLKIN2	I	Level Shift Clock 2 Input
20	CLKIN1	I	Level Shift Clock 1 Input
21	STVIN	I	Level Shift STV Input
22	CLKOUT1	I/O	Level Shift Clock 1 Output
23	CS_1	I/O	Clock 1 Charge-Sharing Input
24	CLKOUT2	I/O	Level Shift Clock 2 Output
25	CS_2	I/O	Clock 2 Charge-Sharing Input
26	CLKOUT3	I/O	Level Shift Clock 3 Output
27	CS_3	I/O	Clock 3 Charge-Sharing Input
28	CLKOUT4	I/O	Level Shift Clock 4 Output
29	EP		The exposed pad must be soldered to a large PCB and connected to VGL1 for maximum power dissipation

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

The AAT1922 provides 8 channel level shifters to drive the TFT LCD panels with row drivers integrated on the panel glass. In addition, the device contains two output specifically intended for discharging the LCD panel during power-down. The device includes various system protection schemes such as input under-voltage lockout (UVLO) and over temperature protection (OTP).

Under Voltage Lockout on VGH

For systematic startup, AAT1922 employs a UVLO rising threshold of 15V typical. Thus, the input supply voltage (V_{GH}) must exceed the UVLO threshold for reliable operation. When V_{GH} is below the UVLO Threshold, all output signals will be clamped to its respective negative supply, V_{GL1} or V_{GL2}, to avoid improper operation at low input voltages.

Over Temperature Protection (OTP)

The device enters into fault protection shutdown when the junction temperature reaches approximately 150°C. When junction temperature cooling down, the device will restart all of the scan-driver outputs again.

Panel Discharge (DISCH1 & DISCH2)

The AAT1922 includes a function for discharging the display panel during power-down. The discharge function comprises a comparator and two level shifters (DISCH1 & DISCH2) which are grouped for different low-level supplies. DISCH1 channel is supplied from VGL1, and DISCH2 channel is supplied from VGL2. VGL1 and VGL2 can be connected together. In typical application, the input supply (V_{GH}) is monitored by connecting a resistive divider from the input to ground, with center tap connected to DIS_SENSE. During normal operation, the voltage applied to the DIS_SENSE pin is greater than V_{REF}, the outputs of the level shifter DISCH1 & DISCH2 are at V_{GL1} and V_{GL2} respectively. During power-down, When the DIS_SENSE voltage is lower than the threshold voltage (V_{REF}) of 1.20V, both of outputs (DISCH1 & DISCH2) must be pulled high to track V_{GH} as their discharge immediately and simultaneously. As shown in AAT1922 Functional Block Diagram, use the following equation to calculate the required resistors of R1 and R2.

$R1=R2x((V_{GH}/V_{REF})-1)$ where $V_{REF}=1.20V$, $R2=10k\Omega$

Level Shifter Output Control

The states of the STVOUT, RESETOUT, and CLKOUT1 ~CLKOUT6 outputs are determined by the corresponding input logic levels present on STVIN, RESETIN, and CLKIN1~CLKIN6 respectively.

STVIN is the synchronous signal for picture frames, and its frequency depends on frame rate. The STVOUT signal follows the STVIN input signal.

For GOA circuit, a reset signals (RESETOUT) are needed. RESETOUT will follow RESETIN and have transients between V_{GH} and V_{GL1}.

The states of the CLKOUT1~CLKOUT6 outputs are determined by the input logic levels present on CLKIN1 ~CLKIN6 which are the synchronous signals for horizontal lines, and their frequency depends on frame rate and vertical resolution. The CLKOUT1~CLKOUT6 channels are all included charge-sharing function which features to shape the corner of the scan-driver output in order to reduce flicker for improving TFT LCD image quality and power consumption.

Charge-Sharing Function Setting (SEL_CS)

The charge-sharing function of the CLKOUT1~CLKOUT6 scan drives can be disable when SEL_CS pin is between 0V to 0.5V, the Timing Chart as shown in Figure 3, when SEL_CS pin is set between 1V to 2V, the charge-sharing mode 1 will be enable, as shown in Figure 4, and when SEL_CS pin is set between 2.8V to 5.5V, that will operate in the charge-sharing mode 2, as shown in Figure 5. Note that when the SEL_CS pin is left floating, the charge-sharing function is still disabled via an internal pull-low circuit.

Power On/Off Sequence

The AAT1922 Power On/Off Sequence is as shown in Figure 1. When power up, the internal reference is ready, all of the level-shifter scan-driver outputs (STVOUT, CLKOUT1~CLKOUT6, RESETOUT, DUSCH1) should follow VGL1 level except panel discharge output DISCH2 will follow VGL2. Once the V_{GH} exceeds the UVLO (V_{GH_UVLO}) threshold, the device enters into normal operation. The 8 channel scan-driver outputs swing is according to their corresponding input logic levels, the voltage applied to the DIS_SENSE pin is greater than V_{REF}, the discharge outputs of the level shifter (DISCH1 & DISCH2) are at V_{GL1} and V_{GL2} respectively.

During power off, when the DIS_SENSE voltage is lower than the threshold voltage (V_{REF}) of typical 1.20V, All of the level-shifter scan-driver outputs (STVOUT, CLKOUT1~CLKOUT6, RESETOUT, DISCH1 and DISCH2) must be pulled high to track V_{GH} as their discharge immediately and simultaneously. In case the discharge-sense (DIS_SENSE) voltage stays high during power down, all clock output channels follow their input signals until VGH falls below its typical falling UVLO threshold voltage of 3.5 V, then all clock output channels follow VGL1. The discharge channels follow VGL1 and VGL2 all the time. If the discharge function triggered by the falling edge of the discharge-sense (DIS_SENSE) voltage is not used, the DIS_SENSE terminal must be pulled above its maximum threshold voltage of 1.26 V all the time (for example, to 3.3 V).

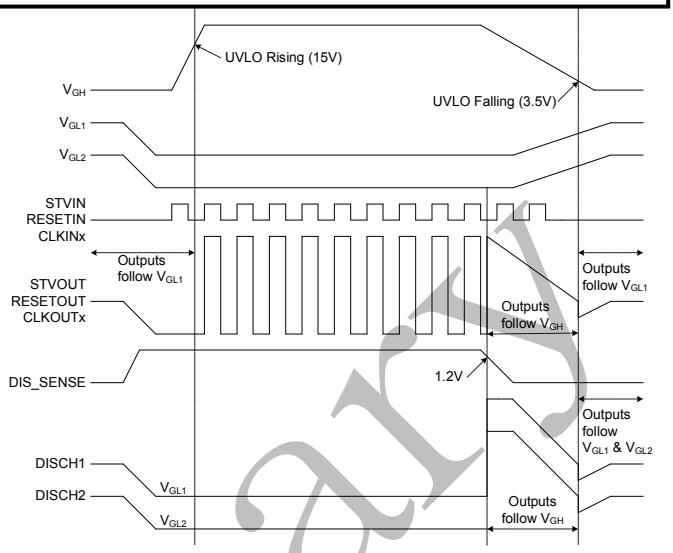


Figure 1. AAT1922 Power On/Off Sequence

STVIN1 Logic Chart

Input			Output
STVIN	**CLKINx**	**RESETIN**	**STVOUT**
High	x	x	VGH
Low	x	x	VGL1
x: Don't Care			

CLKOUTx and Charge-Sharing Logic Chart

Input				Output	
Charge-Sharing Option	**CLKINx**	**STVIN**	**RESETIN**	**CLKOUTx**	**Charge Sharing**
V_{SEL_CS} = 1V~2V & 2.8V~5.5V	High	**x**	x	VGH	No
	Low	Low	x	Hi_Z	Yes
	Low	High	x	VGL1	No
V_{SEL_CS} = 0V~0.5V	High	x	x	VGH	No
	Low	x	x	VGL1	No
x: Don't Care					

Charge-Sharing Mode 0

Charge-sharing disabled (SEL_CS < 0.5 V)

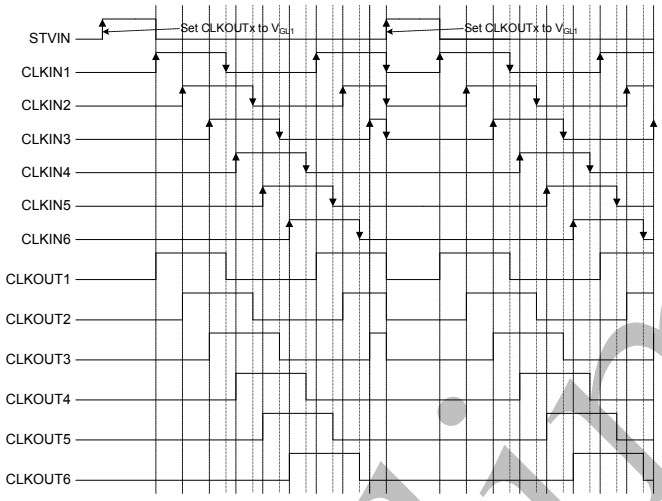


Figure 2. Timing Chart (Without Charge-Sharing Function)

Charge-Sharing Mode 1

Charge-sharing enabled (SEL_CS =1V~2V)

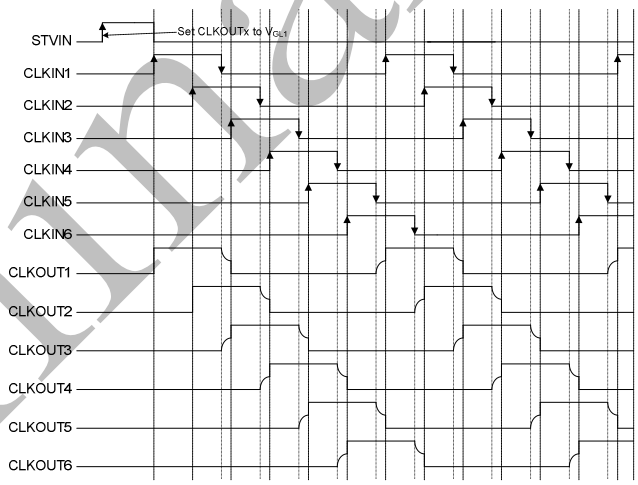


Figure 3. Timing Chart (Charge-Sharing Mode 1)

Charge-sharing of CLKOUT1 ↔ CLKOUT3 between CLKIN1↓ CLKIN3↑.
Charge-sharing of CLKOUT3 ↔ CLKOUT5 between CLKIN3↓ CLKIN5↑.
Charge-sharing of CLKOUT5 ↔ CLKOUT1 between CLKIN5↓ CLKIN1↑.
Charge-sharing of CLKOUT2 ↔ CLKOUT4 between CLKIN2↓ CLKIN4↑.
Charge-sharing of CLKOUT4 ↔ CLKOUT6 between CLKIN4↓ CLKIN6↑.
Charge-sharing of CLKOUT6 ↔ CLKOUT2 between CLKIN6↓ CLKIN2↑.

Charge-Sharing Mode 2

Charge-sharing enabled (SEL_CS =2.8V~6.5V)

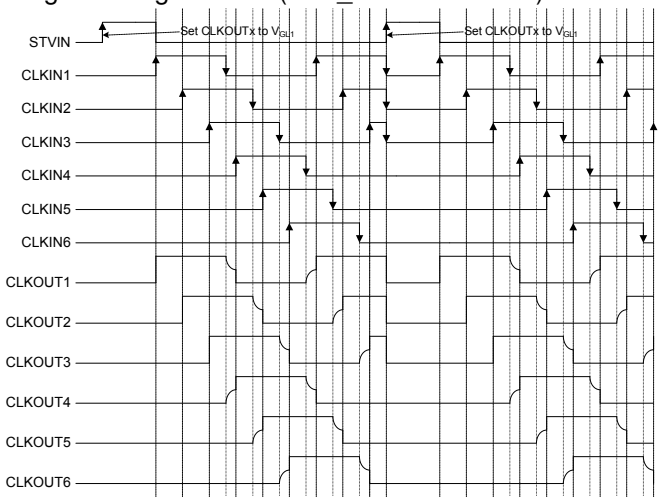


Figure 4. Timing Chart (Charge-Sharing Mode 2)

Charge-Sharing of CLKOUT1 ↔ CLKOUT4 between CLKIN1↓ CLKIN4↑ and CLKIN4↓ CLKIN1↑.
Charge-Sharing of CLKOUT2 ↔ CLKOUT5 between CLKIN2↓ CLKIN5↑ and CLKIN5↓ CLKIN2↑.
Charge-Sharing of CLKOUT3 ↔ CLKOUT6 between CLKIN3↓ CLKIN6↑ and CLKIN6↓ CLKIN3↑.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1922.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VGH, VGL1, VGL2 pin. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VGH, VGL1, VGL2 bypass capacitor should refer to analog ground (GND).

Output Capacitors

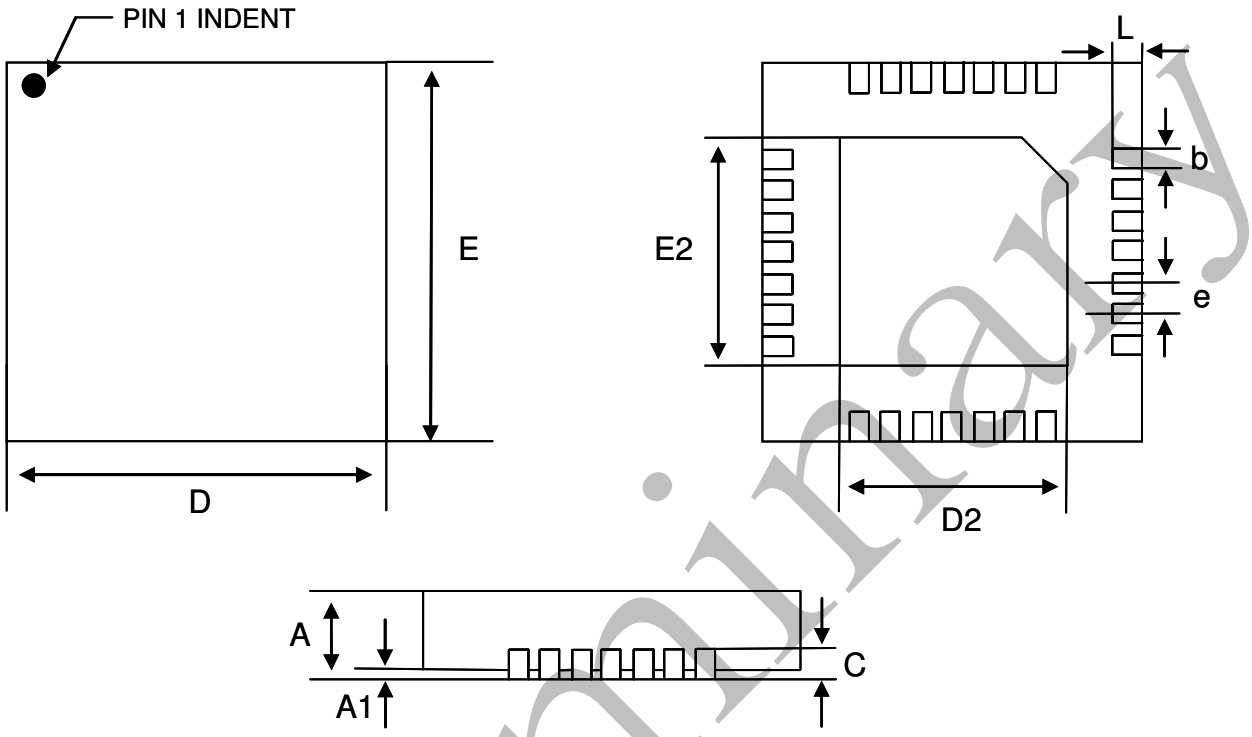
The output stages of the AAT1922 are capable of sinking and sourcing high peak currents that are greater than 500mA in typical applications, the high rates of change of current occurring at the rising and falling edges of each output require stray inductance to be minimized. This can be achieved by minimize the trace length and maximize the trace width between the STVOUT, RESRETOUT, DISCH1, DISCH2, and CLKOUT1~CLKOUT6 output nodes to minimize the parasitic inductance and its load for best transient response.

Ground Plane

Connect the exposed pad of IC's bottom side to the VGL1 copper plane, and the copper plane area should be maximized to improve thermal dissipation.

PACKAGE DIMENSION

WQFN28-4X4



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
C	---	0.20	---
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e	-----	0.40	-----
L	0.35	0.40	0.45