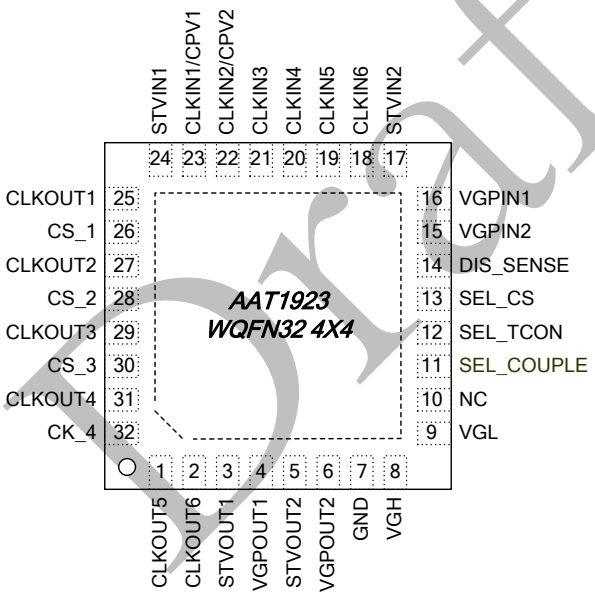
LEVEL SHIFTER FOR TFT LCD GOA PANEL

10-CHANNEL LEVEL SHIFTER WITH CHARGE-SHARING AND PANEL DISCHARGE

FEATURES

- 2-Channel STVOUTx Outputs for STVINx
- 2-Channel VGPOUTx Outputs for VGPINx
- 6-Channel CLKOUTx Outputs for CLKINx
  - Charge-Sharing Mode Selectable
  - TCON Mode Selectable
  - Clock Decouple Mode Selectable
- Level-Shifter Supply Voltage Range
  - Max. +45V for High Level (VGH)
  - Min. -20V for Low Level (VGL)
- Panel Discharge
- Protection
  - Under-Voltage Lockout (UVLO)
  - Over Temperature Protection (OTP)
- WQFN32-4x4 Package Available

PIN CONFIGURATION



GENERAL DESCRIPTION

The AAT1923 contains 10 channel level-shifter scan drivers which are designed to drive the TFT panels with row drivers integrated on the panel glass. Each level-shifter scan-driver can swing from +45V to -20V and features low impedance output stages that achieve fast rise and fall times even when driving the capacitive loading typically present in LCD display applications.

The level-shifter scan-driver outputs (STVOUT1, STVOUT2, VGPOUT1, VGPOUT2, and CLKOUT1 ~CLKOUT6) converts the logic-level signals generated by the Timing Controller (T-CON) to the high-level signals used by the display panel. And the clock outputs (CLKOUTx) support two TCON Mode, three charge -sharing mode, and three clock decouple mode selections for improving TFT LCD image quality and power consumption.

The panel discharge function is used to monitor the device supply voltage via DIS_SENSE pin. It works with the integrated voltage detector. When system power down, the voltage detector will command all of the level-shifter scan-driver outputs to swing to VGH so as to remove residual image quickly.

The AAT1923 provides various protection mechanisms such as input under-voltage lockout (UVLO) and over temperature protection. The device is available in a small WQFN 32 pin 4x4x0.75mm with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40°C to +85°C temperature range.

APPLICATIONS

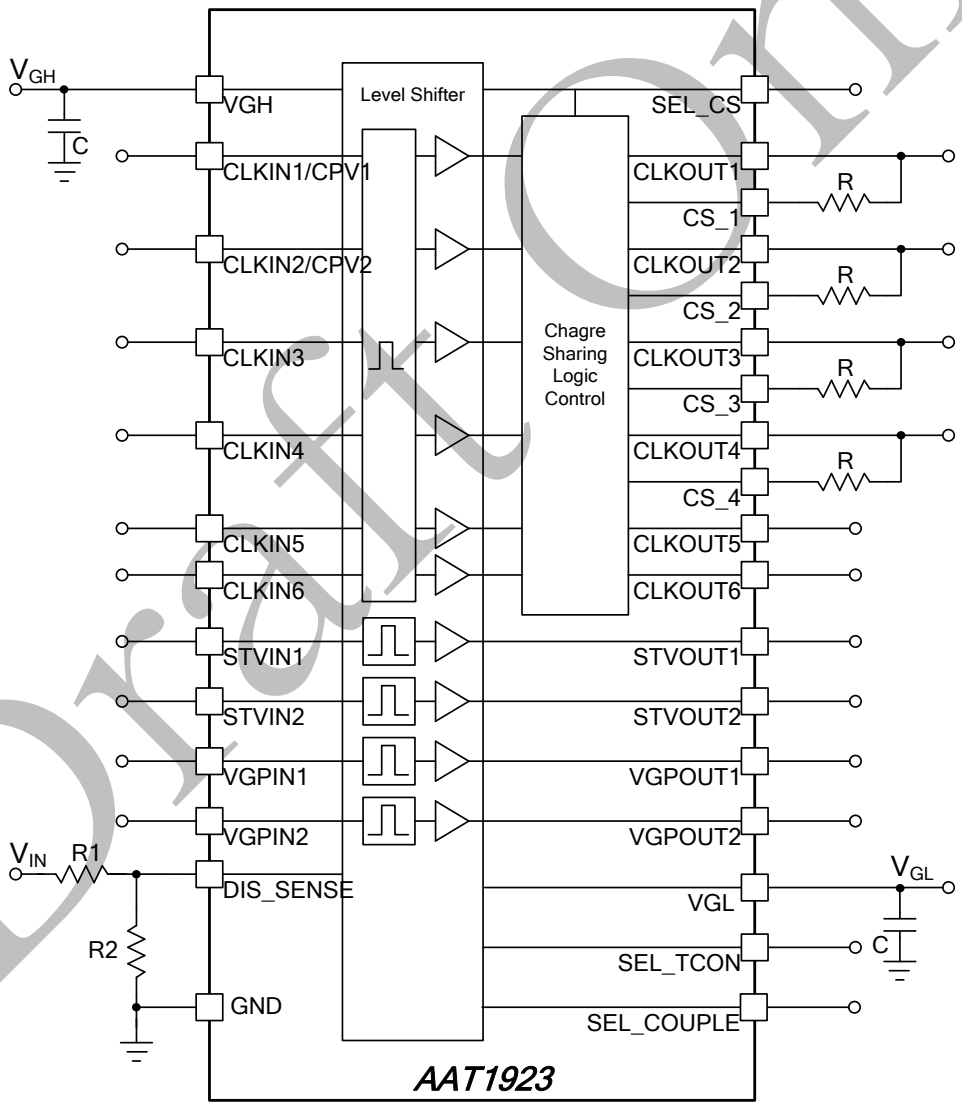
- TFT LCD GOA Panel

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1923	AAT1923-Q30-T	Q30:WQFN 32-4x4	T: Tape and Reel	−40°C to +85°C	1923 XXXXX XXXX	Device Type Lot no. (4~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VGH to GND	V_{GH}	-0.3 to +50	V
VGL to GND	V_{GL}	-20 to +0.3	V
VGH to VGL	V_{GH-L}	60	V
Input Voltage (STVIN1, STVIN2, CLKIN1/CPV1, CLKIN2/CPV2, CLKIN3, CLKIN4, CLKIN5, CLKIN6, VGPIN1, VGPIN2, DIS_SENSE, SEL_CS, SEL_TCON, SEL_TCON)	V_I	-0.3 to +6.0	V
Output Voltage (STVOUT1, STVOUT2, CLKOUT1, CLKOUT2, CLKOUT3, CLKOUT4, CLKOUT5, CLKOUT6, CS_1, CS_2, CS_3, CS_4, VGPOUT1, VGPOUT2)	V_O	$-0.3-V_{GL}$ to $V_{GH}+0.3$	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	-65 to +150	°C
Package Thermal Range	θ_{JA}	27.8	°C / W
Power Dissipation @ T_A = +25°C , T_J = +125°C	P_d	3.59	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{GH} = 30V, V_{GL} = -10V, GND = 0V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VGH Input Voltage Range	V_{GH}	V_{GH}–V_{GL}<60V	16.5	-	45	V
VGL Input Voltage Range	V_{GL}	V_{GH}–V_{GL}<60V	-18	-	-3	V
Operating Frequency CPV1/CPV2	f_{OSC}			500		kHz
V_{GH}–V_{GL} Voltage Range	V_{GH}–V_{GL}		-	-	60	V
VGH Quiescent Current	I_{Q_VGH}		-	0.8	-	mA
VGL Quiescent Current	I_{Q_VGL}		-	0.37	-	mA
VGH Under Voltage Lockout Threshold	V_{GH_UVLO}	Rising	14	15	16	V
		Falling	2	3.5	5.0	V
Thermal Shutdown	T_{SHDN}		130	150	170	°C

ELECTRICAL CHARACTERISTICS

(V_{GH} = 30V, V_{GL} = -10V, GND = 0V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature)

Input Signals (STVIN1, CLKINx, VGPINx, DIS_SENSE, SEL_CS)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Low level Input Voltage	V_{IL}		-	-	0.8	V
High level Input Voltage	V_{IH}		2	-	-	V
Input Bias Current	I_B		-40	-	+40	nA
Charge-Sharing threshold voltage	V_{SEL_CS}	Disable	0	-	0.5	V
		Enable, Mode 1	1	-	2	
		Enable, Mode 2	2.8		5	
SEL_CS Internal Pull-Low Resistor	R_{SEC_CS}	V_{SEL_CS} =3.3V	50	100	200	kΩ
Decouple Mode Selection threshold	V_{SEL_COUPLE}	Disable CK Decouple	0	-	0.5	V
		CK Decouple, Mode 1	1	-	2	
		CK Decouple, Mode 2	2.8		5	
SEL_COUPLE Internal Pull-Low Resistor	R_{SEC_COUPLE}	V_{SEL_COUPLE} =3.3V	50	100	200	kΩ
TCON Mode Selection threshold	V_{SEL_TCON}	TCON Mode1	0		0.8	V
		TCON Mode2	2		5	
SEL_TCON Internal Pull-Low Resistor	R_{SEC_TCON}	V_{SEL_TCON} =3.3V	50	100	200	kΩ
Input Current (STVIN, CLKINx, VGPIN, DIS_SENSE)	I_{IN}	CLKINx=STVIN=5V, VGPIN=DIN_SENSE=5 V	-	2	100	µA
Input Current (SEL_CS)		SEL_CS=5V,	-	50	100	µA
Level Shifter Input Pull Low Resistance	R_{IN}		50	100	200	kΩ
Discharge threshold voltage	V_{REF}		1.14	1.20	1.26	V

ELECTRICAL CHARACTERISTICS

(V_{GH} = 30V, V_{GL} = -10V, GND = 0V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature)

Level Shifter Outputs (STVOUT1&2, VGPOUT1&2, CLKOUTx, CS_x)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
STVOUT1&2, VGPOUT1&2, CLKOUTx Rising Propagation Delay Time	T_{RPD}	C_{OUT}=150pF	-	40	100	ns
STVOUT1&2, VGPOUT1&2, CLKOUTx Falling Propagation Delay Time	T_{FPD}	C_{OUT}=150pF	-	50	100	ns
CLKOUTx Rising Charge Sharing Propagation Delay Time	t_{RPD_CS}	C_{OUT}=150pF, R_{CS}=50Ω	-	50	150	ns
CLKOUTx Falling Charge Sharing Propagation Delay Time	t_{FPD_CS}	C_{OUT}=150pF, R_{CS}=50Ω	-	70	150	ns
STVOUT1&2, VGPOUT1&2 Slew Rate	SR+	C_{OUT}=4.7nF, V_{OUT}=20% to 80%	20	50		V/µs
	SR-		30	60	-	V/µs
CLKOUTx Slew Rate	SR+	C_{OUT}=4.7nF, V_{OUT}=20% to 80%	50	140		V/µs
	SR-		50	150	-	V/µs
Internal charge-sharing resistance	R_{CS}	I_{LOAD}=10mA	30	60	100	Ω
CLKOUTx High-Side Switch-On Resistance	r_{DSON_H1}	I_{OUT}=10mA, sourcing (high side)	-	14	30	Ω
CLKOUTx Low-Side Switch-On Resistance	r_{DSON_L1}	I_{OUT}=-10mA, Sinking (low side)	-	14	30	Ω
STVOUT1&2, VGPOUT1&2 High-Side Switch-On Resistance	r_{DSON_H1}	I_{OUT}=10mA, sourcing (high side)	-	30	60	Ω
STVOUT1&2, VGPOUT1&2 Low-Side Switch-On Resistance	r_{DSON_L1}	I_{OUT}=-10mA, Sinking (low side)	-	15	30	Ω

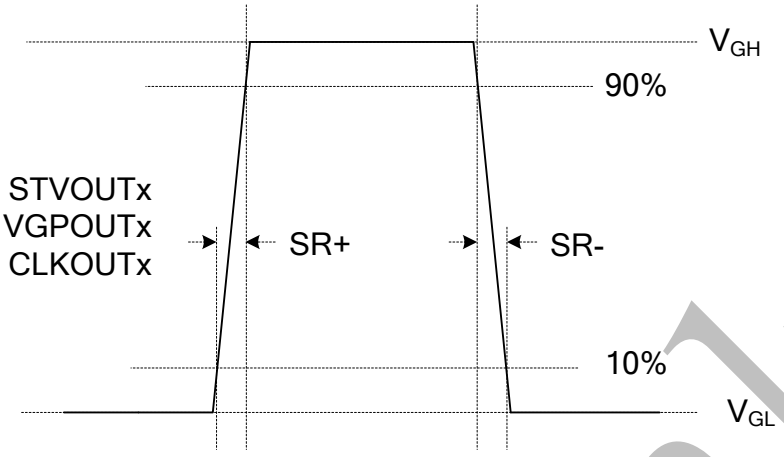


Figure A. Rising and Falling Time

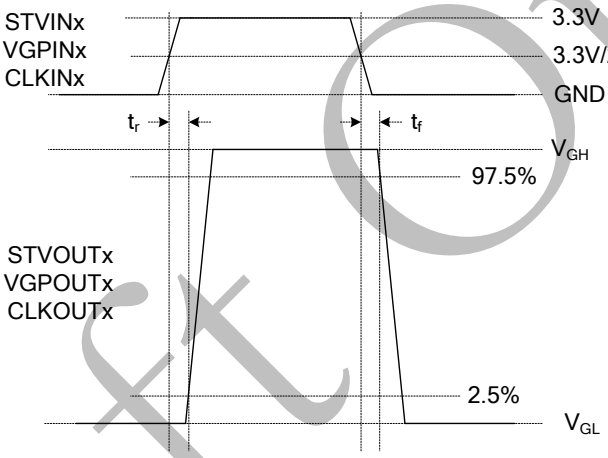


Figure B. Propagation Delay

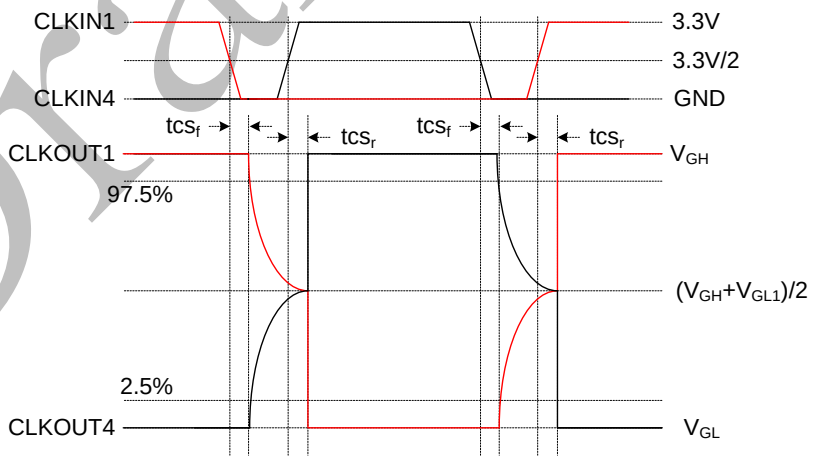
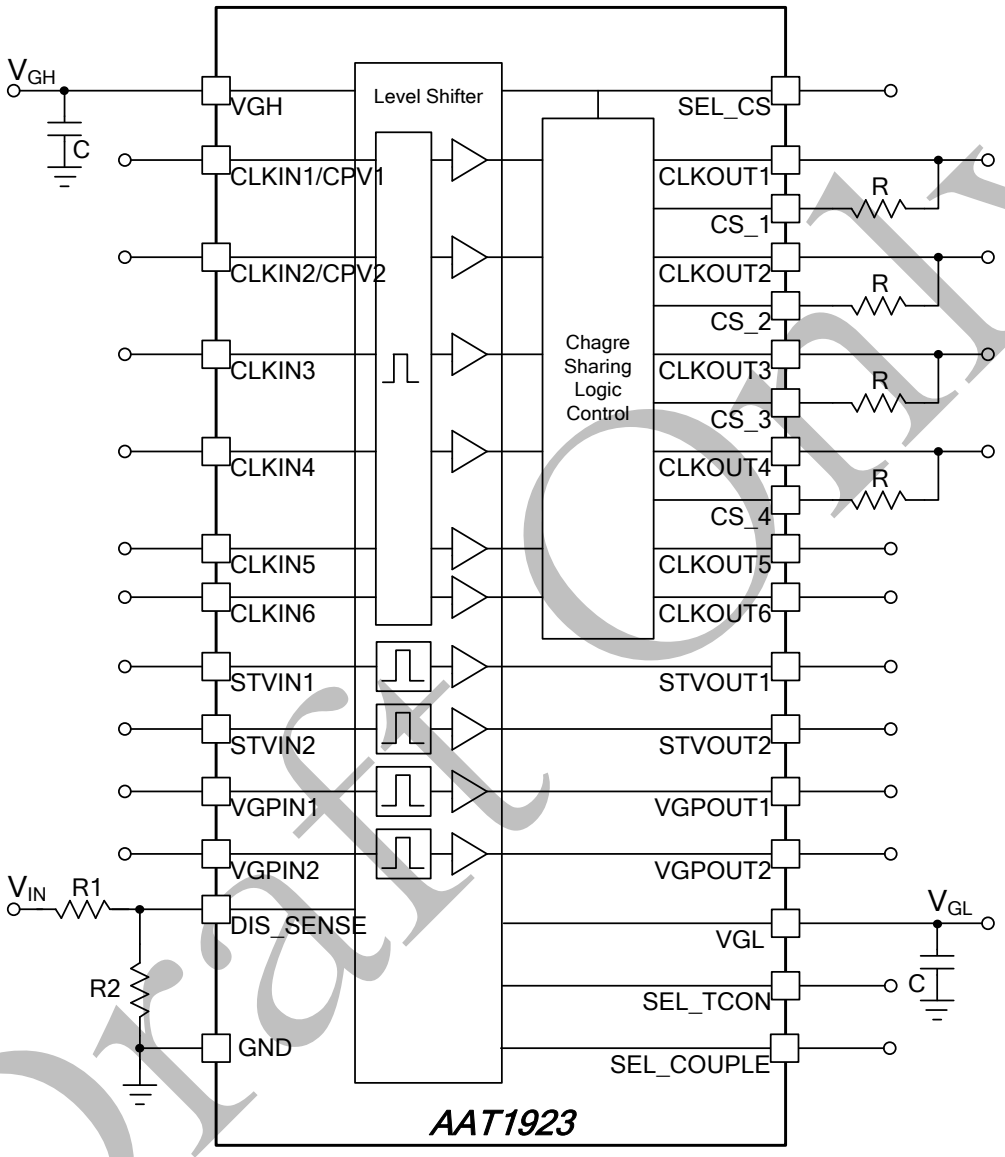


Figure C. Charge-Sharing of Propagation Delay

PIN DESCRIPTION

PIN NO	NAME	I/O	DESCRIPTION
1	CLKOUT5	O	Level Shift Clock 5 Output
2	CLKOUT6	O	Level Shift Clock 6 Output
3	STVOUT1	O	Level Shift STV1 Output
4	VGPOUT1	O	Level Shift VGP1 Output
5	STVOUT2	O	Level Shift STV2 Output
6	VGPOUT2	O	Level Shift VGP2 Output
7	GND	-	Ground
8	VGH	P	Positive Supply Voltage Input
9	VGL	P	Negative Supply Voltage Input
10	NC	-	No Connect
11	SEL_COUPLE	I	Decouple Mode Selection
12	SEL_TCON	I	TCON Mode Selection
13	SEL_CS	I	Charge-Sharing Mode Selection
14	DIS_SENSE	I	Discharge Sensing Voltage Pin
15	VGPIN2	I	Level Shift VGP2 Input
16	VGPIN1	I	Level Shift VGP1 Input
17	STVIN2	I	Level Shift STV2 Input
18	CLKIN6	I	Level Shift Clock 6 Input
19	CLKIN5	I	Level Shift Clock 5 Input
20	CLKIN4	I	Level Shift Clock 4 Input
21	CLKIN3	I	Level Shift Clock 3 Input
22	CLKIN2/CPV2	I	Level Shift Clock 2 Input, CLKIN2 for TCON Mode 1, CPV2 for TCON Mode 2
23	CLKIN1/CPV1	I	Level Shift Clock 1 Input, CLKIN1 for TCON Mode 1, CPV1 for TCON Mode 2
24	STVIN1	I	Level Shift STV1 Input
25	CLKOUT1	I/O	Level Shift Clock 1 Output
26	CS_1	I/O	Clock 1 Charge-Sharing Input
27	CLKOUT2	I/O	Level Shift Clock 2 Output
28	CS_2	I/O	Clock 2 Charge-Sharing Input
29	CLKOUT3	I/O	Level Shift Clock 3 Output
30	CS_3	I/O	Clock 3 Charge-Sharing Input
31	CLKOUT4	I/O	Level Shift Clock 4 Output
32	CS_4	I/O	Clock 4 Charge-Sharing Input
33	Exposed Pad		Connect to VGL, The exposed pad must be soldered to a large PCB and connected to VGL for maximum power dissipation.

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

The AAT1923 provides 10 channel level-shifter scan-drivers to drive the TFT LCD panels with row drivers integrated on the panel glass. In addition, the device contains the panel discharge function to monitor the device supply voltage for discharging the LCD panel during power-down. The device includes various system protection schemes such as input under-voltage lockout (UVLO) and over temperature protection (OTP).

Under Voltage Lockout on VGH

For systematic startup, AAT1923 employs a UVLO rising threshold of 15V typical. Thus, the input supply voltage (V_{GH}) must exceed the UVLO threshold for reliable operation. When V_{GH} is below the UVLO Threshold, all output signals will be clamped to its respective negative supply (V_{GL}) to avoid improper operation at low input voltages.

Over Temperature Protection (OTP)

The device enters into fault protection shutdown when the junction temperature reaches approximately 150°C. When junction temperature cooling down, the device will restart all of the scan-driver outputs again.

Panel Discharge (DIS_SENSE)

The AAT1923 includes a function for discharging the display panel during power-down. In typical application, the input supply (V_{GH}) is monitored by connecting a resistive divider from the input to ground, with center tap connected to DIS_SENSE. During normal operation, the voltage applied to the DIS_SENSE pin is greater than V_{REF}, During power-down, When the DIS_SENSE voltage is lower than the threshold voltage (V_{REF}) of 1.26V, all of scan-driver outputs (STVOUT1, STVOUT2, CLKOUT1~CLKOUT6, VGPOUT1, VGPOUT2) must be pulled high to track V_{GH} as their discharge immediately and simultaneously. As shown in Figure 1. AAT1923 Power On/Off Sequence, use the following equation to calculate the required resistors of R_1 and R_2.

$R_1=R_2x((V_{GH}/V_{REF})-1)$ where $V_{REF}=1.26V$, $R_2=10k\Omega$

Level-Shifter Scan-Diver Outputs

The AAT1923 contains 10 channel level-shifter scan-drivers which are designed to drive the TFT panels with row drivers integrated on the panel glass. The high-voltage level-shifter scan-drivers feature a logic-level input stage and a high-level output stage that can swing from +45V (maximum) to -20V (minimum), and a combined maximum range of $V_{GH} – V_{GL}$ = 60V.

STVOUT1, STVOUT2, VGPOUT1, and VGPOUT2 Outputs

The states of the STVOUT1, STVOUT2, VGPOUT1, and VGPOUT2 outputs are determined by the input logic levels present on STVIN1, STVIN2, VGPIN1, and VGPIN2. STVIN1 and STVIN2 are the synchronous signals for picture frames, and their frequency depends on frame rate. The STVOUT1 and STVOUT2 signals follow the STVIN1 and STVIN2 input signals respectively.

For GOA circuit, the VGP signals (VGPOUT1 and VGPOUT2) are needed. VGPOUT1 and VGPOUT2 will follow VGPIN1, VGPIN2 respectively, and have transients between V_{GH} and V_{GL}.

CLKOUT1~CLKOUT6 Outputs

The CLKOUT1~CLKOUT6 are the synchronous signals for horizontal lines, and their frequency depends on frame rate and vertical resolution.

TCON Mode Selection (SEL_TCON)

The states of the CLKOUT1~CLKOUT6 outputs are determined by the setting of TCON mode. At TCON mode 1 (TM1), the corresponding input logic levels present on CLKIN1~CLKIN6 will control the states of the CLKOUT1~CLKOUT6 outputs respectively. When the TCON mode is set 2 (TM2), the CLKOUT1~CLKOUT6 outputs go high on the rising edge of CPV1 (CLKIN1/CPV1 pin) and go low on the rising edge of CPV2 (CLKIN2/CPV2 pin).

Charge-Sharing Mode Setting (SEL_CS)

The CLKOUT1~CLKOUT6 channels are all included charge-sharing function which features to shape the corner of the scan-driver output in order to reduce flicker for improving TFT LCD image quality and power consumption.

The charge-sharing function of the CLKOUT1~CLKOUT6 scan-drives can be disable when SEL_CS pin is between 0V to 0.5V (CSM0), the Timing Chart as shown in Figure 3, when SEL_CS pin is set between 1V to 2V (CSM1), the charge-sharing mode 1 will be enable, as shown in Figure 4, and when SEL_CS pin is set between 2.8V to 5.5V (CSM2), that will operate in the charge-sharing mode 2, as shown in Figure 5. Note that when the SEL_CS pin is left floating, the charge-sharing function is still disabled via an internal pull-low circuit.

Power On/Off Sequence

The AAT1923 Power On/Off Sequence is as shown in Figure 1. When power up, the internal reference Voltage is ready, all of the level-shifter scan-driver outputs (STVOUT1, STVOUT2, CLKOUT1~CLKOUT6, VGPOUT1, VGPOUT2) should follow VGL level. Once the V_{GH} exceeds the UVLO (V_{GH_UVLO}) threshold, the device enters into normal operation. At TCON mode 1 (TM1), the 10 channel scan-driver outputs swing is according to their corresponding input logic levels respectively. And at TCON mode 2 (TM2), the six clock outputs (CLKOUTx) will control by CLKIN1/CPV1 and CLKIN2/CPV2, and the other four level-shifter scan-driver outputs (STVOUT1, STVOUT2, VGPOUT1, VGPOUT2) swing is according to their corresponding input logic levels respectively.

During power off, when the DIS_SENSE voltage is lower than the threshold voltage (V_{REF}) of typical 1.2V, All of the level shifter scan-driver outputs (STVOUT1, STVOUT2, CLKOUT1~CLKOUT6, VGPOUT1, VGPOUT2) must be pulled high to track V_{GH} as their discharge immediately and simultaneously. In case the discharge-sense (DIS_SENSE) voltage stays high during power down, all clock output channels follow their input signals until VGH falls below its typical falling UVLO threshold voltage of 3.5 V, then all clock output channels follow VGL. Note that the discharge function triggered by the falling edge of the discharge-sense (DIS_SENSE) voltage is not used, the DIS_SENSE terminal must be pulled above its maximum threshold voltage of 1.26 V all the time (for example, to 3.3 V).

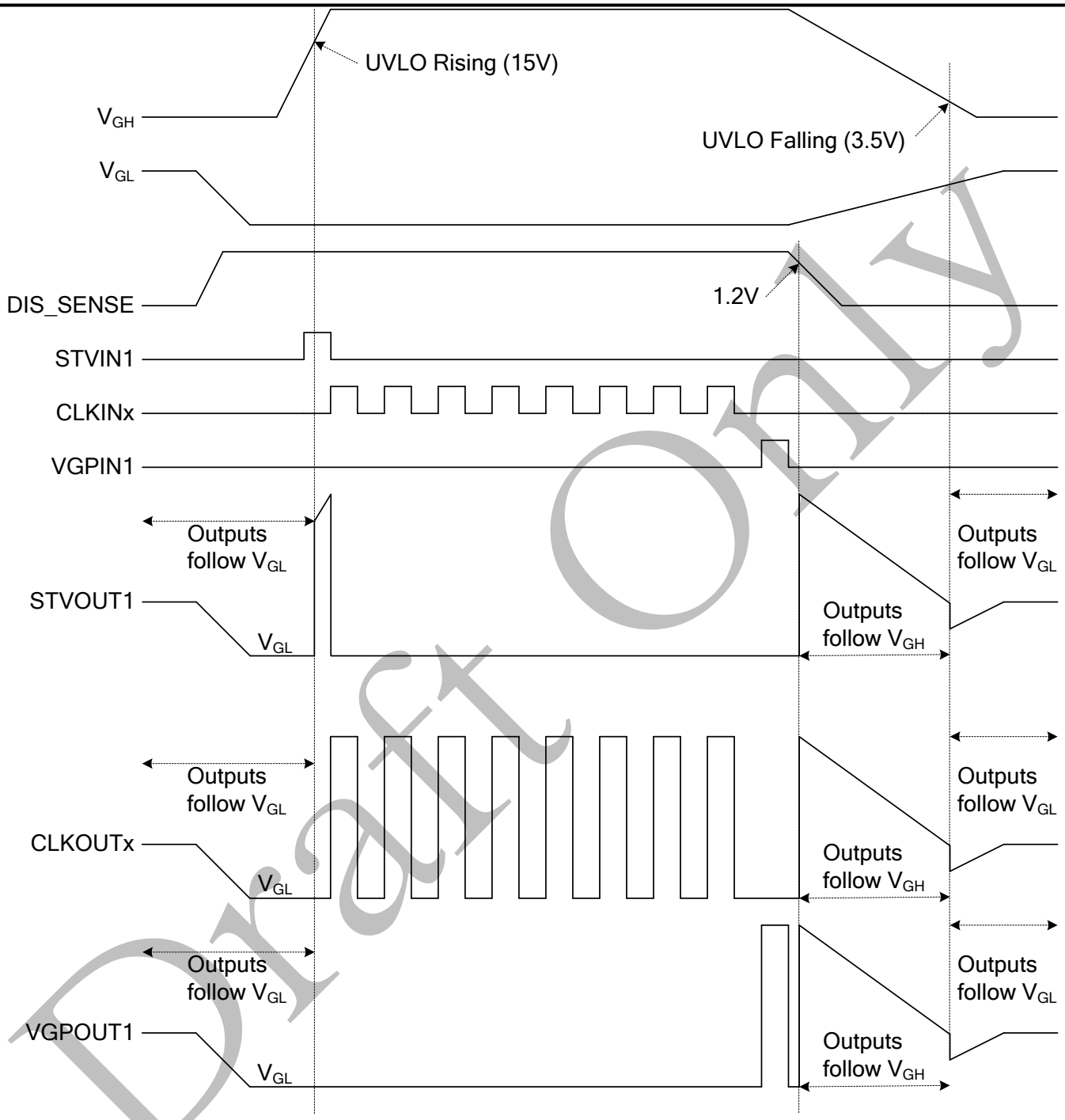


Figure 1. AAT1923 Power On/Off Sequence

STVIN1 Logic Chart

Input			Output
STVIN1	**CLKINx**	**VGPIN1**	**STVOUT1**
High	x	x	VGH
Low	x	v	VGL
x: Don't Care			

CLKOUTx and Charge-Sharing Logic Chart

Input				Output	
Charge-Sharing Option	**CLKINx**	**STVIN1**	**VGPIN1/2**	**CLKOUTx**	**Charge Sharing**
V_{SEL_CS} = 1V~2V & 2.8V~5.5V	High	**x**	x	VGH	No
	Low	Low	x	Hi_Z	Yes
	Low	High	x	VGL	No
V_{SEL_CS} = 0V~0.5V	High	x	x	VGH	No
	Low	x	x	VGL	No
x: Don't Care					

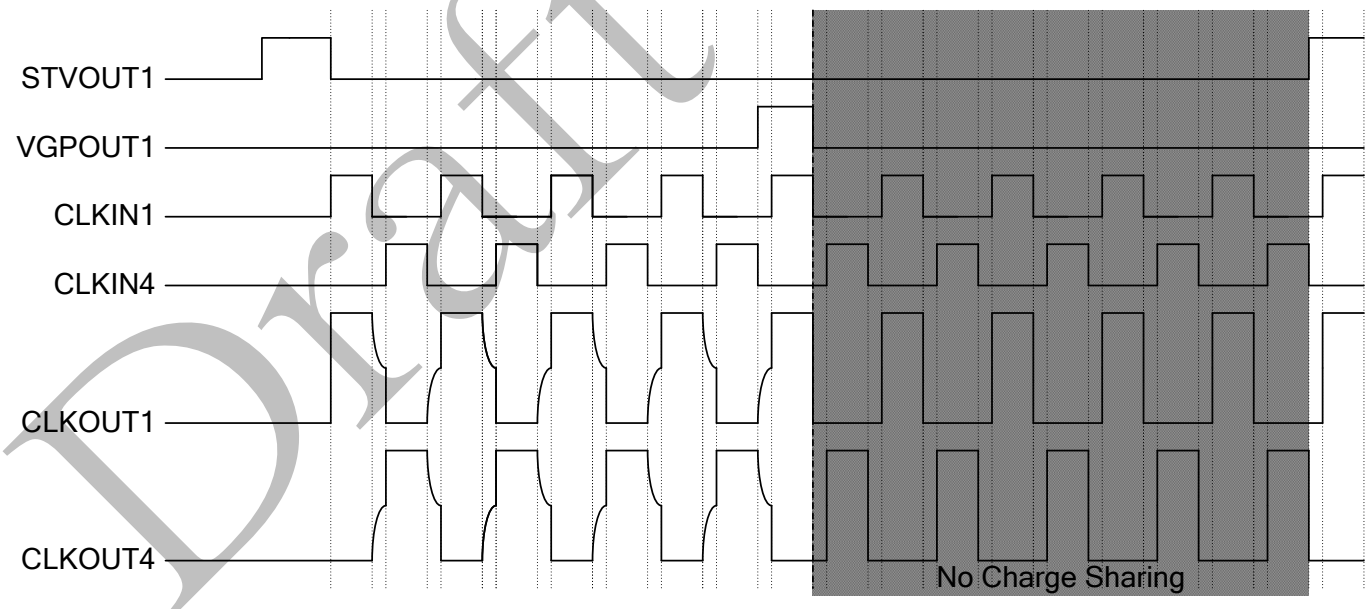


Figure 2. Frame Start / End Timing

TCON Mode 1 (TM1) & Charge-Sharing Mode 0 (CSM0)

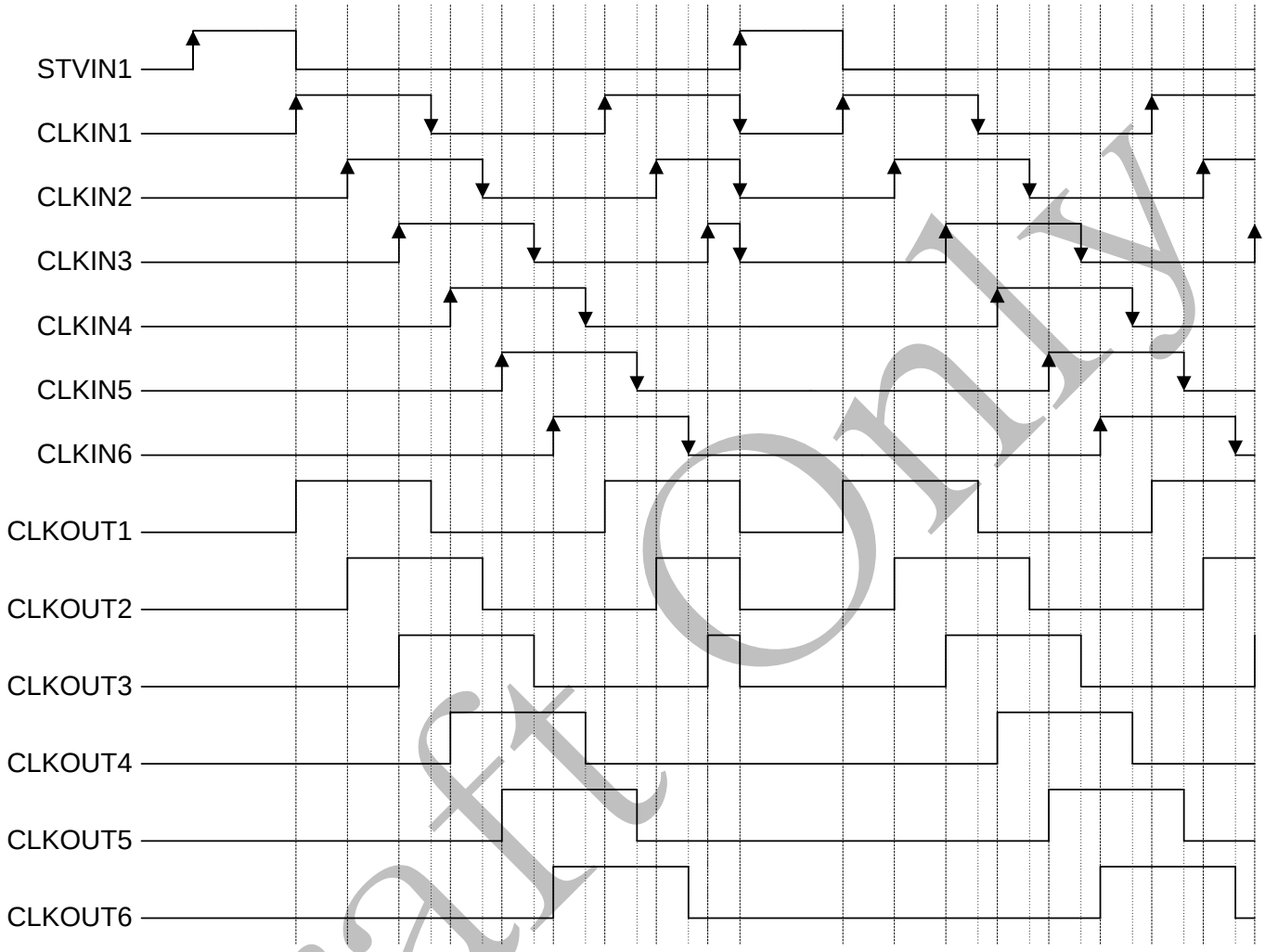


Figure 3. Timing Chart (TCON Mode1, Charge-Sharing Mode 0)

TCON Mode 1 (TM1) & Charge-Sharing Mode 1 (CSM1)

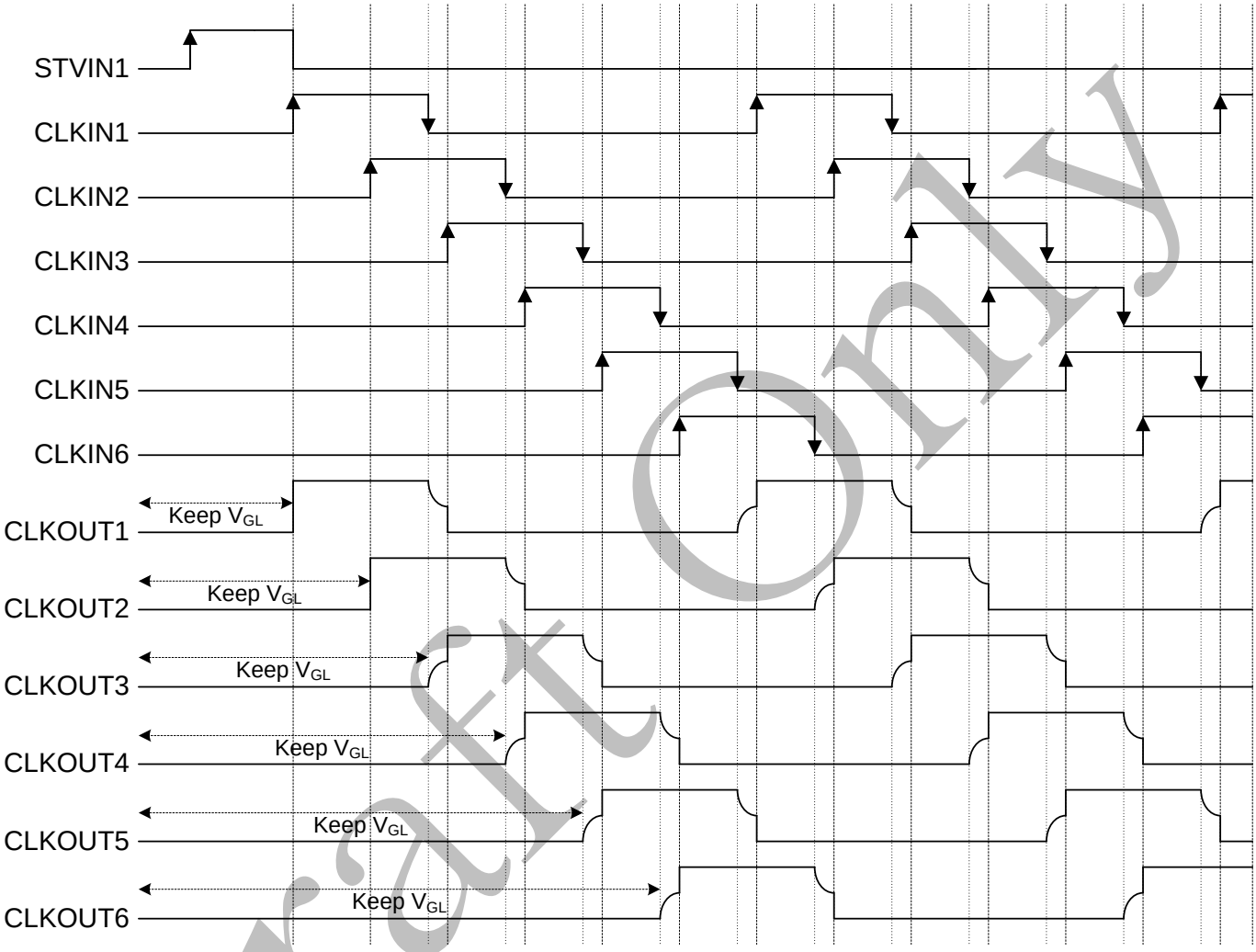


Figure 4. Timing Chart (TCON Mode1, Charge-Sharing Mode 1)

1. Charge-sharing of CLKOUT1 ↔ CLKOUT3 between CLKIN1↓ CLKIN3↑.
2. Charge-sharing of CLKOUT3 ↔ CLKOUT5 between CLKIN3↓ CLKIN5↑.
3. Charge-sharing of CLKOUT5 ↔ CLKOUT1 between CLKIN5↓ CLKIN1↑.
4. Charge-sharing of CLKOUT2 ↔ CLKOUT4 between CLKIN2↓ CLKIN4↑.
5. Charge-sharing of CLKOUT4 ↔ CLKOUT6 between CLKIN4↓ CLKIN6↑.
6. Charge-sharing of CLKOUT6 ↔ CLKOUT2 between CLKIN6↓ CLKIN2↑.

TCON Mode 1 (TM1) & Charge-Sharing Mode 2 (CSM2)

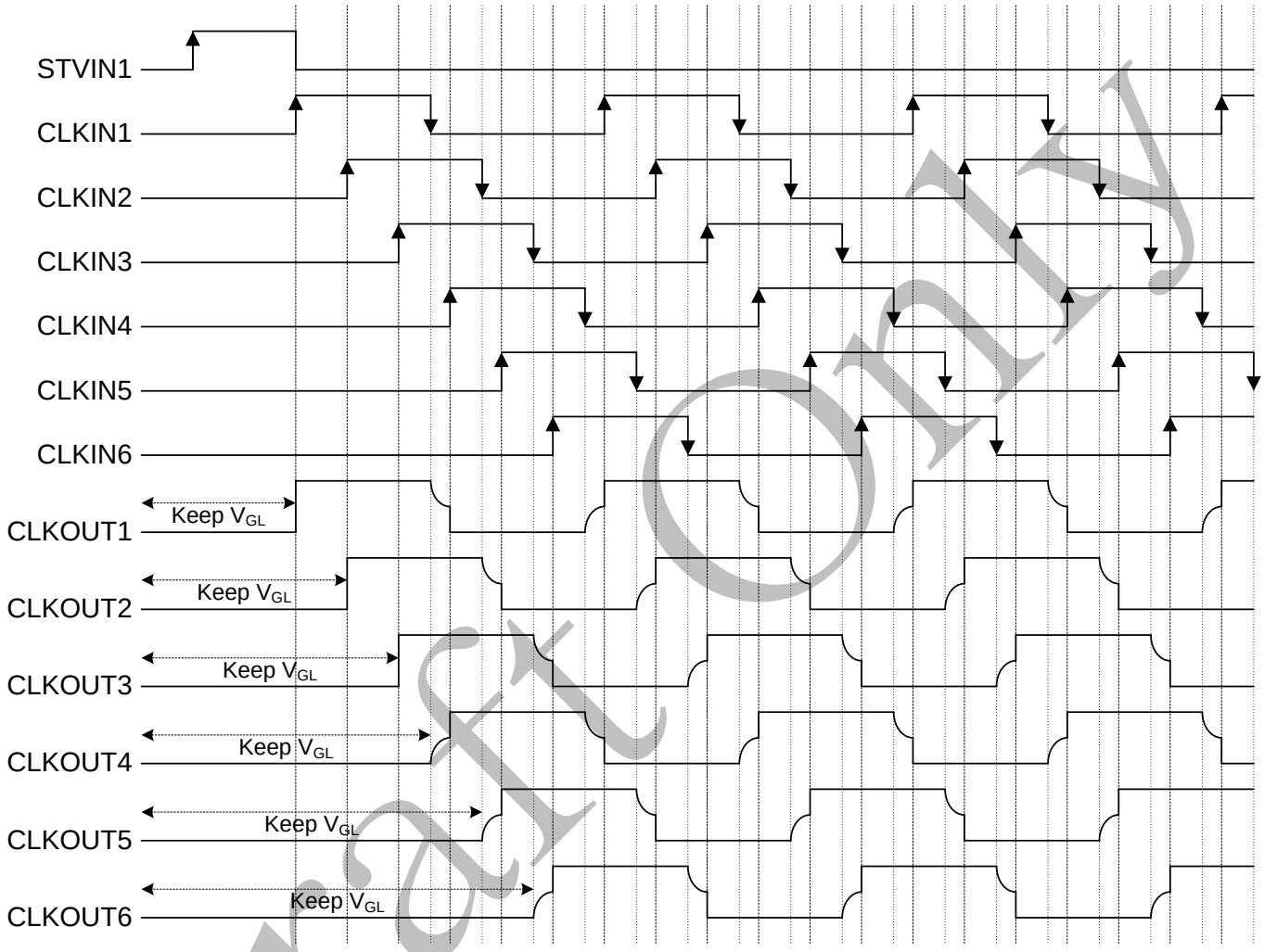


Figure 5. Timing Chart (TCON Mode1, Charge-Sharing Mode 2)

1. Charge-Sharing of CLKOUT1 ↔ CLKOUT4 between CLKIN1↓ CLKIN4↑ and CLKIN4↓ CLKIN1↑.
2. Charge-Sharing of CLKOUT2 ↔ CLKOUT5 between CLKIN2↓ CLKIN5↑ and CLKIN5↓ CLKIN2↑.
3. Charge-Sharing of CLKOUT3 ↔ CLKOUT6 between CLKIN3↓ CLKIN6↑ and CLKIN6↓ CLKIN3↑.

TCON Mode 2 (TM2) & Charge-Sharing Mode 0 (CS0)

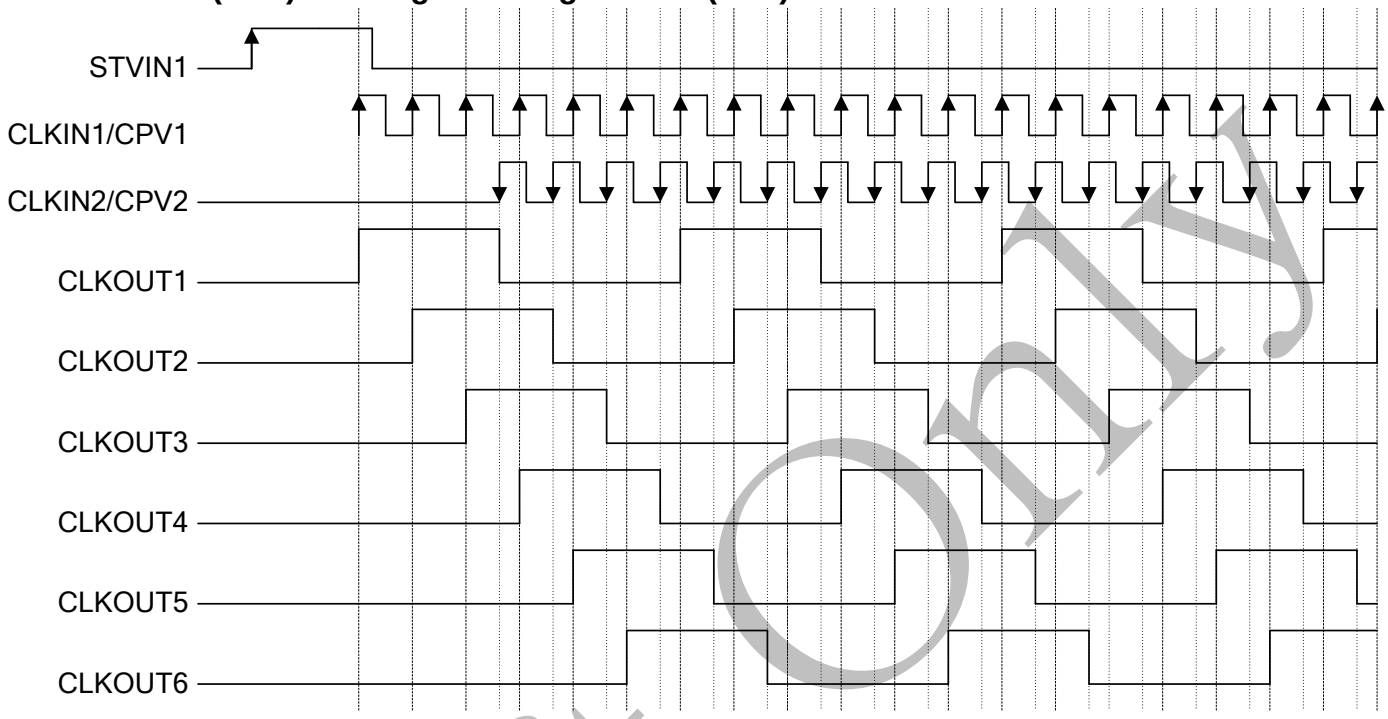


Figure 6. Timing Chart (TCON Mode2, Charge-Sharing Mode 0)

TCON Mode 2 (TM2) & Charge-Sharing Mode 1 (CSM1)

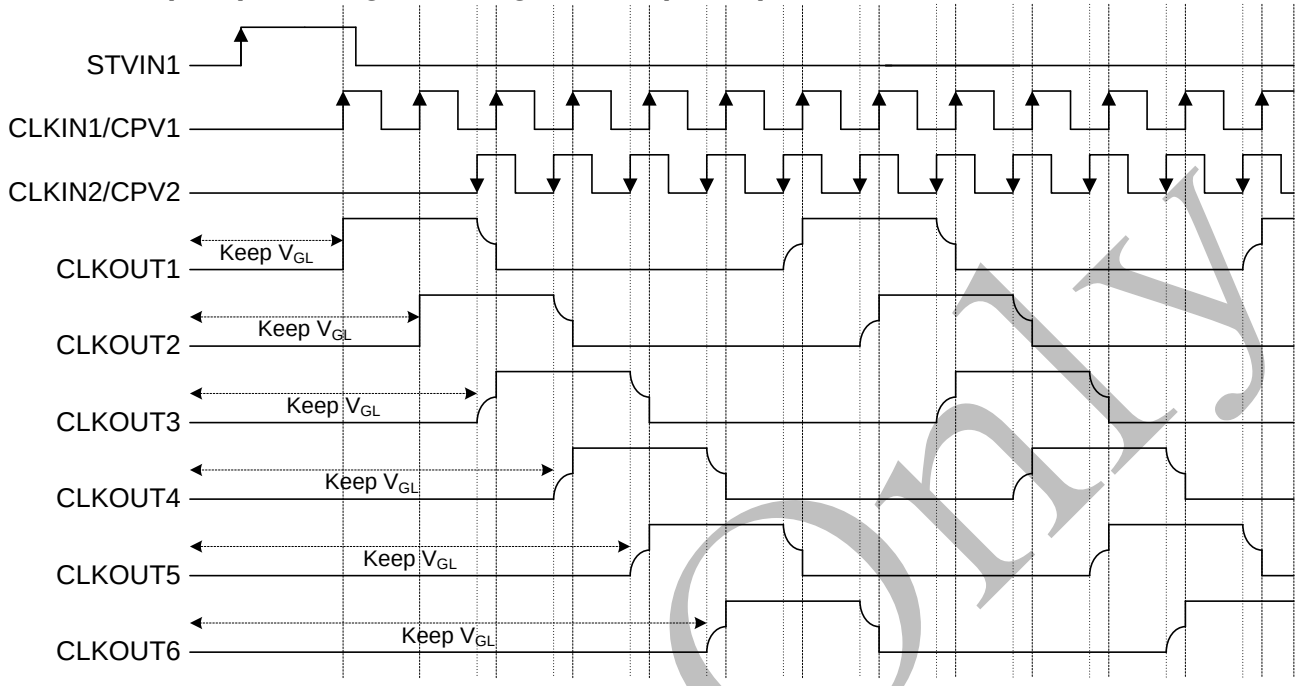


Figure 7. Timing Chart (TCON Mode2, Charge-Sharing Mode 1)

TCON Mode 2 (TM2) & Charge-Sharing Mode 2 (CSM2)

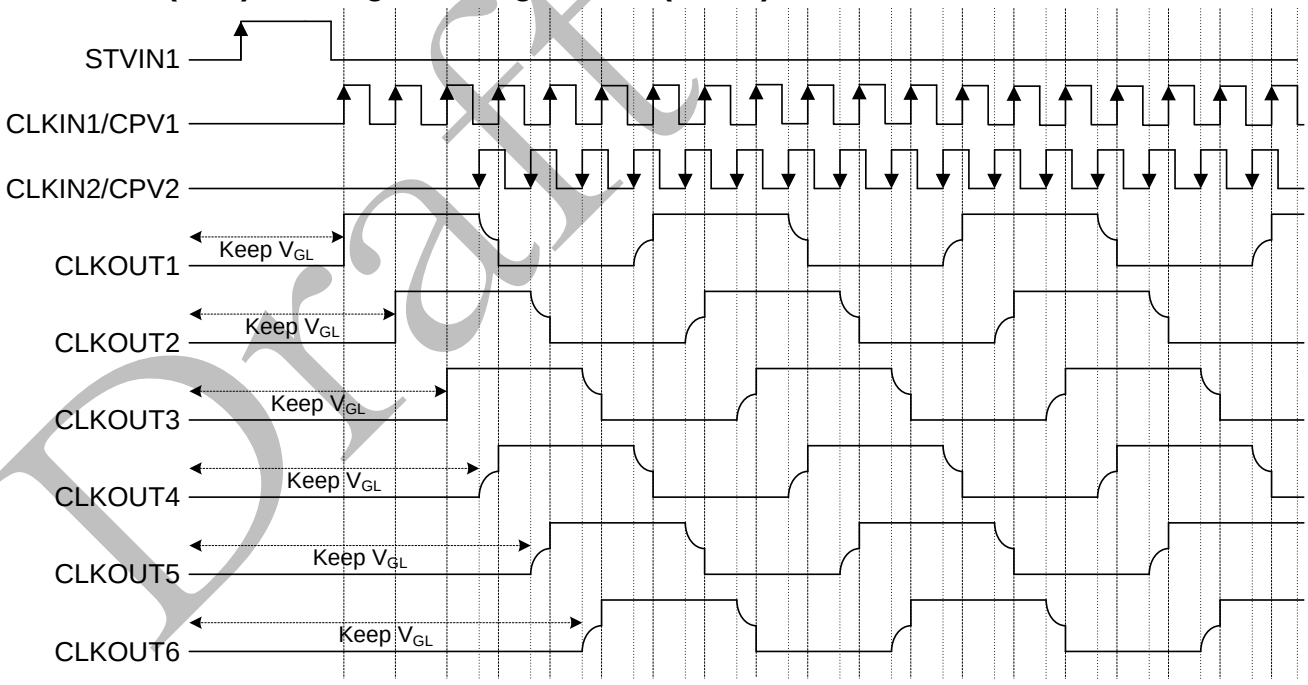


Figure 8. Timing Chart (TCON Mode2, Charge-Sharing Mode 2)

TCON Mode 2 (TM2) & Charge-Sharing Mode1 (CSM1) & Decouple Mode 0 (DM0)

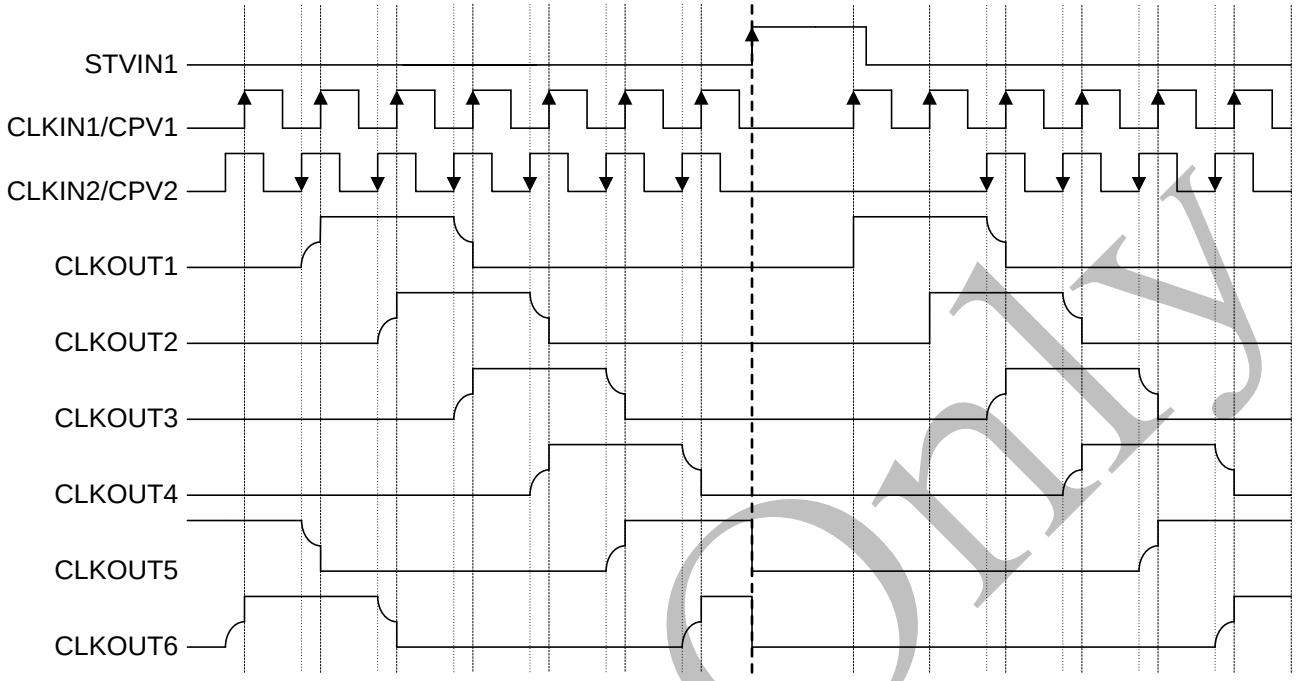


Figure 9. Timing Chart (TCON Mode2, Charge-Sharing Mode 1, Decouple Mode 0)
STVIN1 rising, CLKOUT1~6 pull low

TCON Mode 2 (TM2) & Charge-Sharing Mode 2 (SCM2) & Decouple Mode 0 (DM0)

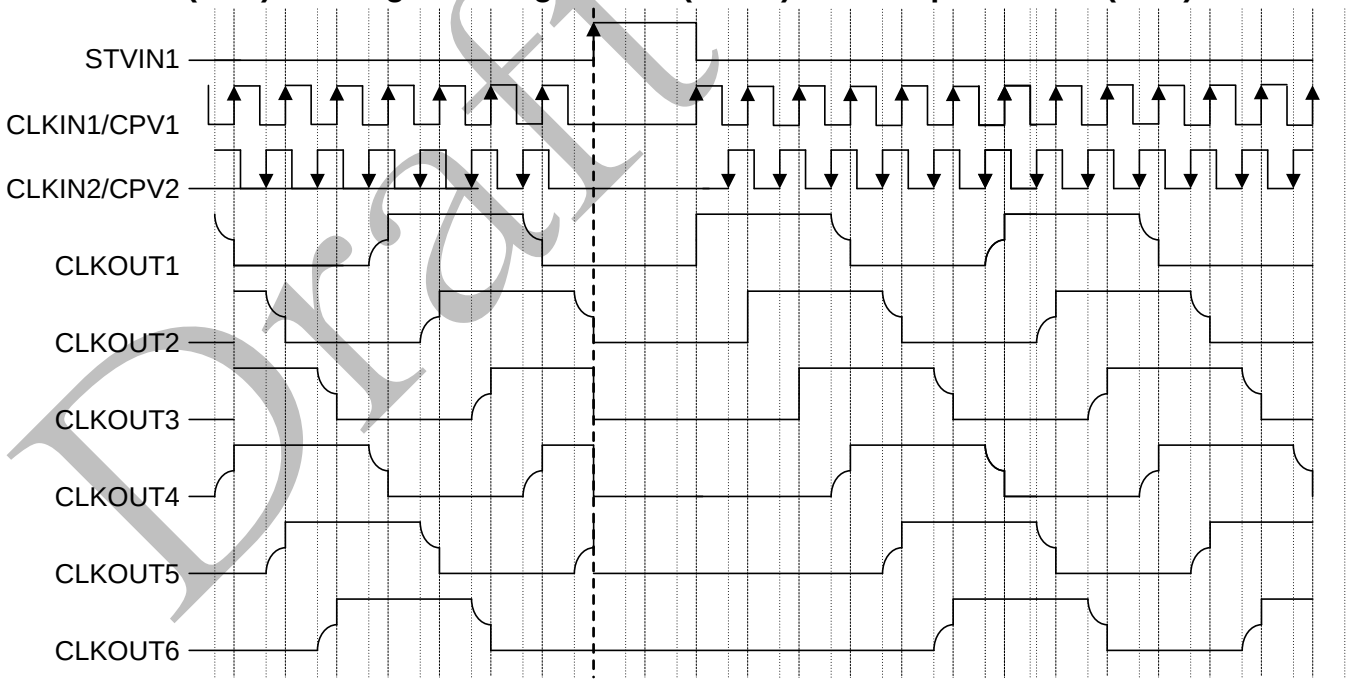


Figure 10. Timing Chart (TCON Mode2, Charge-Sharing Mode 2, Decouple Mode 0)
STVIN1 rising, CLKOUT1~6 pull low

TCON Mode 2 (TM2) & Charge-Sharing Mode 1 (CSM1) & Decouple Mode 1 (DM1)

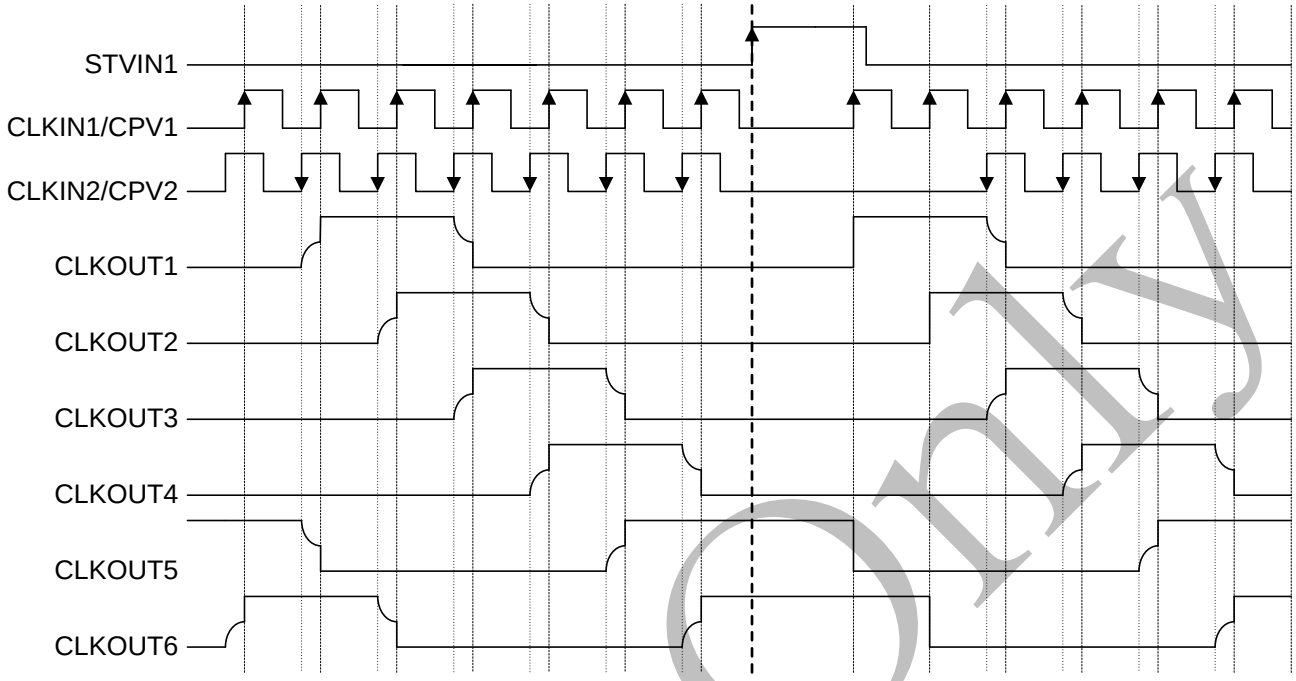


Figure 11. Timing Chart (TCON Mode2, Charge-Sharing Mode 1, Decouple Mode 1)

STVIN1 rising, CLKOUT1~4 pull low
CLKOUT5 is falling when CLKOUT1 is rising
CLKOUT6 is falling when CLKOUT2 is rising

TCON Mode 2 (TM2) & Charge-Sharing Mode 2 (CSM2) & Decouple Mode 2 (DM2)

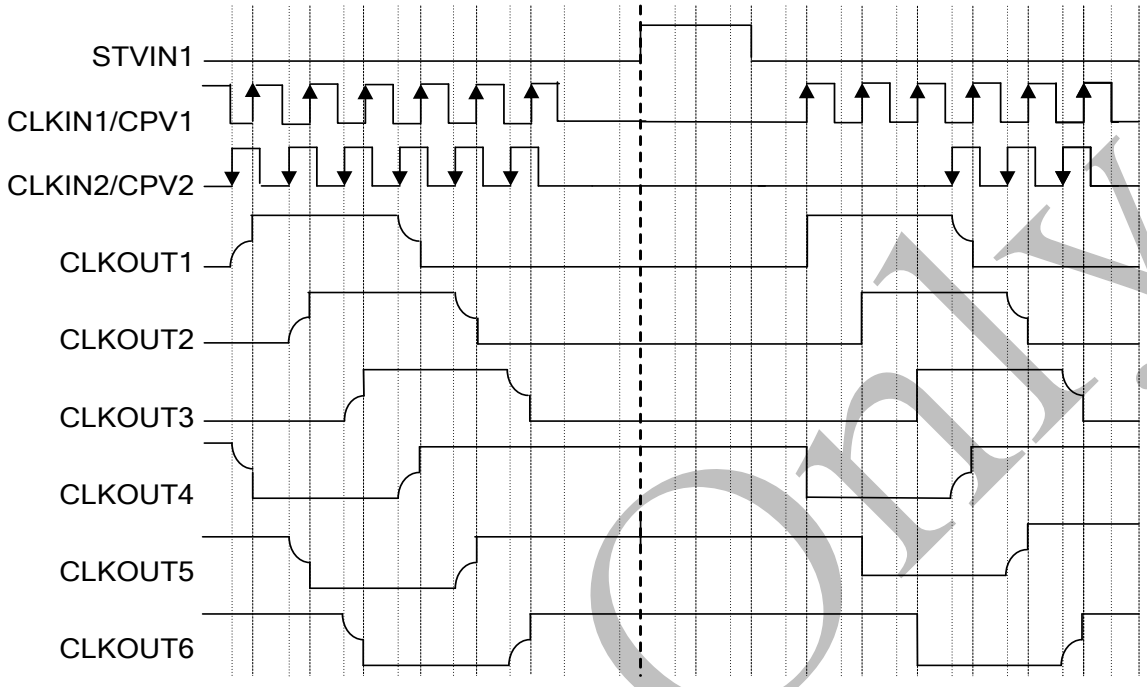


Figure 12. Timing Chart (TCON Mode2, Charge-Sharing Mode 2, Decouple Mode 2)

STVIN1 rising, CLKOUT1~3 pull low
CLKOUT4 is falling when CLKOUT1 is rising
CLKOUT5 is falling when CLKOUT2 is rising
CLKOUT6 is falling when CLKOUT3 is rising

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1923.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VGH and VGL pin. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VGH and VGL bypass capacitor should refer to analog ground (GND).

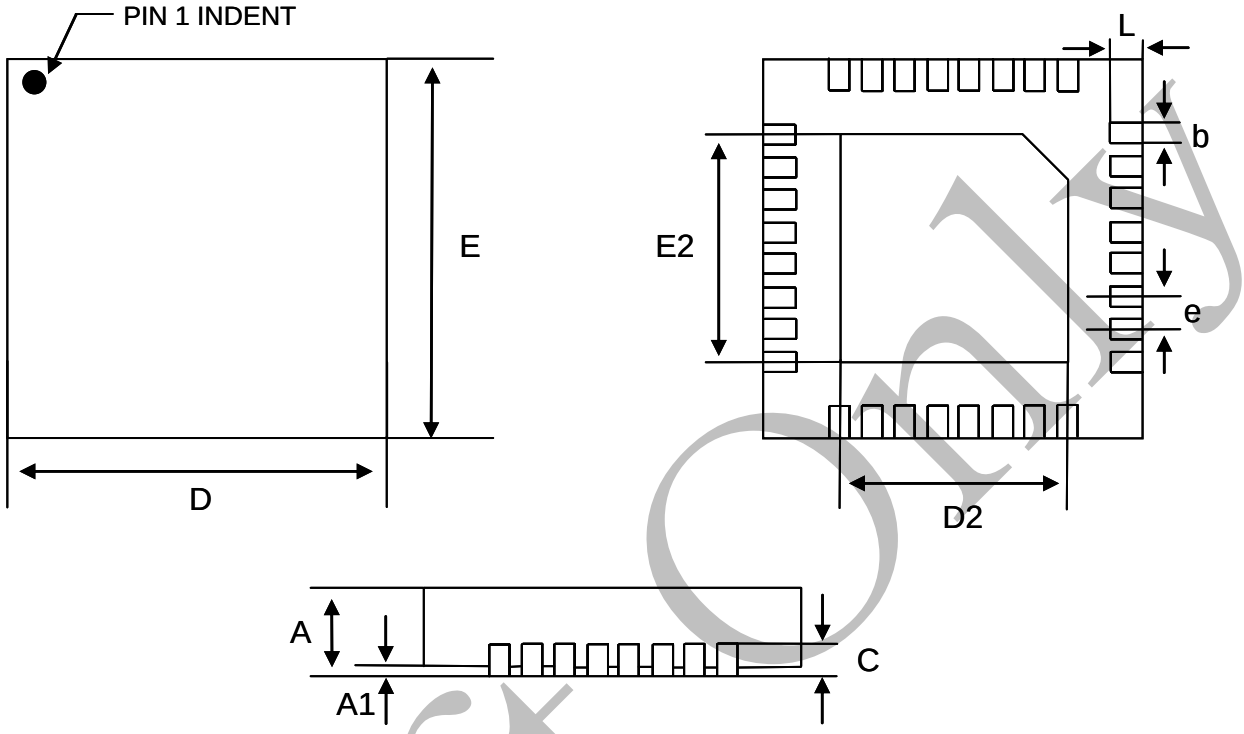
Output Capacitors

The output stages of the AAT1923 are capable of sinking and sourcing high peak currents that are greater than 500mA in typical applications, the high rates of change of current occurring at the rising and falling edges of each output require stray inductance to be minimized. This can be achieved by minimize the trace length and maximize the trace width between the STVOUT1, STVOUT2, RESRETOUT1, RESRETOUT2, and CLKOUT1~ CLKOUT6 output nodes to minimize the parasitic inductance and its load for best transient response.

Ground Plane

Connect the exposed pad of IC's bottom side to the VGL copper plane, and the copper plane area should be maximized to improve thermal dissipation

PACKAGE DIMENSION



Symbol	Dimensions In Millimeters		
	Min	TYP	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.15	0.2	0.25
C	-----	0.2	-----
D	3.9	4	4.1
D2	2.75	2.8	2.85
E	3.9	4	4.1
E2	2.75	2.8	2.85
e	-----	0.4	-----
L	0.35	0.4	0.45

Package: WQFN32-4X4, Package Code: Q30