AT6861EM

SPEC

V1.9

Date: 2016/12/06

This document contains information on a new product specifications and information herein are subject to change without notice.

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Revision History

Rev.	Date	Author	Description
V1.0	2012/01/11	Dream	Reference: V0.931
V1.1	2013/03/11	Dream	Reference: V0.932
V1.2	2013/03/25	Dream	Reference: V0.933
V1.3	2013/04/16	Dream	Reference: V0.934
V1.4	2013/06/25	Dream	Reference: V0.935
V1.5	2013/12/04	Dream	Reference: V0.936
V1.6	2013/12/06	Dream	Reference: V0.937; Add Pin.55 (SCReserve) Description
V1.7	2014/03/19	Dream	Reference: V0.938; Modify Page 8 ,10 & 11
V1.8	2014/03/20	Dream	Reference: V0.938; Modify Page 10 & 11
V1.9	2016/12/06	Kevin	DAC information modify

1. GENERAL DESCRIPTION:

The AT6861EM Digital Reverb Engine provides high performance digital audio signal processing capability required to implement a compact, easy to use, high quality reverb solution. Built-in SRAM eliminates the need for wide bus connections to external RAM and allows custom development. The 16 embedded programs enable instant usability and general application.

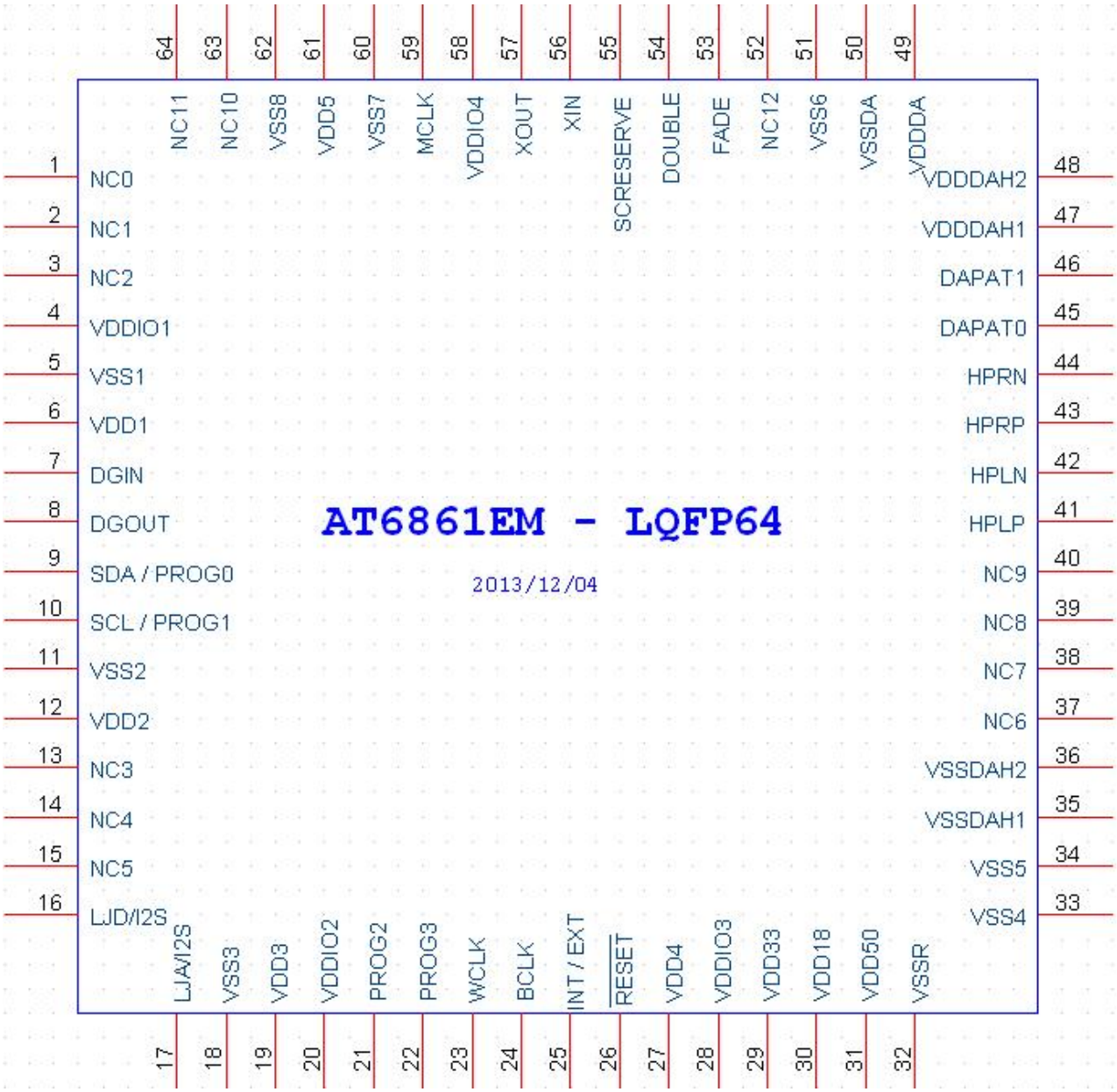
FEATURES:

- 16 selectable functions include halls, rooms, plates, delays, chorus, flange, vocal cancel, and rotary speaker emulation.
- Serially programmable SRAM for program development or dynamically changing programs
- 128 instructions per word clock. (6 MIPS @ 48 kHz Sampling Frequency).
- 32K Word location STATIC RAM provides over 0.68s of delay at 48 kHz sampling frequency.
- Built-in 2 24-bits STEREO 3rd Order DSM-DAC
  [Internal DAC(Pin.41 ~ 44)]
- 4 LFO Engine
- I²S/Left-Justified Interface Selectable
- Distortion Effect Unit
- Fade-in/Fade-out Unit to anti-noise
- Using External12MHz Crystal (The best is 12.288MHz)

Applications:

- Guitar and Instrument Amps
- Digital Mixing Boards
- Karaoke Systems
- Digital Effects Boxes
- Computer Sound Cards
- Car Audio Systems
- Personal Stereo Products

2. Pin Configuration:



AT6861EM LQFP64 Diagram

3. Pin assignment and Function description

LQFP 64	Signal Name	Type	Description
1	NC0	NC	No Connection, Include Pull-Down Resister, Reserve is 0.
2	NC1	NC	No Connection, Include Pull-Down Resister, Reserve is 0.
3	NC2	NC	No Connection, Include Pull-Down Resister, Reserve is 0.
4	V_{DDIO1}	P/I	Digital IO 3.3V Power Input Pin
5	V_{SS1}	G	Digital IO Ground Pin
6	V_{DD1}	P/I	Digital Core 1.8V Power Input Pin
7	DGIN	I	PCM Data Input; Include Pull-Down Resister.
8	DGOUT	O	PCM Data Output
9	SDA/PROG0	I	Serial Interface Data Line Input & Internal Program Select 0 Include Pull-Down Resister, Reserve is 0.
10	SCL/PROG1	I	Serial Interface Clock Line Input & Internal Program Select 1 Include Pull-Down Resister, Reserve is 0.
11	V_{SS2}	G	Digital Core Ground Pin
12	V_{DD2}	P/I	Digital Core 1.8V Power Input Pin
13	NC3	NC	No Connection, Include Pull-Down Resister, Reserve is 0.
14	NC4	NC	No Connection, Include Pull-Down Resister, Reserve is 0.
15	NC5	NC	No Connection, Include Pull-Down Resister, Reserve is 0.
16	LJD / I^2S	I/O	Left-Justified / I^2S DAC PCM Select Input Include Pull-Down Resister. (1:LJ; 0: I^2S) , Reserve is 0
17	LJA / I^2S	I/O	Left-Justified / I^2S ADC PCM Select Input Include Pull-Down Resister. (1:LJ; 0: I^2S) , Reserve is 0
18	V_{SS3}	G	Digital Core Ground Pin
19	V_{DD3}	P/I	Digital Core 1.8V Power Input Pin
20	V_{DDIO2}	P/I	Digital IO 3.3V Power Input Pin
21	PROG2	I	Internal Program Select 2 Include Pull-Down Resister, Reserve is 0.
22	PROG3	I	Internal Program Select 3 Include Pull-Down Resister, Reserve is 0.
23	WCLK	O	PCM Word Clock Output
24	BCLK	O	PCM Bit Clock Output

25	INT / EXT	I	Internal/External Program Select Input; Include Pull-Up resister, Reserve is 1. (1:INT ROM;0:EXT ROM)
26	RESET	I	System Reset pin, Active Low Include Pull-Up Resister.
27	V_{DD4}	P/I	Digital Core 1.8V Power Input Pin
28	V_{DDIO3}	P/I	Digital IO 3.3V Power Input Pin
29	V_{DD33}	P/O	LDO Regulator 3.3V Power Output Pin
30	V_{DD18}	P/O	LDO Regulator 1.8V Power Output Pin
31	V_{DD50}	P/I	LDO Regulator 5.0V Power Input Pin
32	V_{SSR}	P/I	LDO Regulator Ground Pin
33	V_{SS4}	G	Digital Core Ground Pin
34	V_{SS5}	G	Digital IO Ground Pin
35	V_{SSDAH1}	G	DAC Digital Ground Pin for post-driver
36	V_{SSDAH2}	G	DAC Digital Ground Pin for post-driver
37	NC6	NC	No Connection, Reserved To Test
38	NC7	NC	No Connection, Reserved To Test
39	NC8	NC	No Connection, Reserved To Test
40	NC9	NC	No Connection, Reserved To Test
41	HPLP	O	Internal DAC Delta-Sigma Left High Digital Data Output, 24mA Driver
42	HPLN	O	Internal DAC Delta-Sigma Left Low Digital Data Output, 24mA Driver
43	HPRP	O	Internal DAC Delta-Sigma Right High Digital Data Output, 24mA Driver
44	HPRN	O	Internal DAC Delta-Sigma Right Low Digital Data Output, 24mA Driver
45	DAPAT0	I	DAC Delta-Sigma Data Pattern Select Input Include Pull-Down Resister, always setting to “1”.
46	DAPAT1	I	DAC Delta-Sigma Data Pattern Select Input Include Pull-Down Resister always setting to “1”.
47	V_{DDDAH1}	P/I	DAC 3.3V Power Input Pin
48	V_{DDDAH2}	P/I	DAC 3.3V Power Input Pin
49	V_{DDDA}	P/I	DAC 1.8V Power Input Pin
50	V_{SSDA}	G	DAC Digital Ground Pin for pre-driver
51	V_{SS6}	G	Digital Core Ground Pin
52	NC12	NC	No Connection, Include Pull-Up Resister, Reserve is “1”.
53	FADE	I/O	FADE IN/OUT Select Input; Include Pull-Down Resister, Reserve is 0. (0:Effect-ON；1:Effect-OFF = By Pass)

54	DOUBLE	I/O	Double Reverb Enable Input; Include Pull-Down Resister, Reserve is 0. (1:Double Enable；0:Double Disable = Normal)
55	SCRESERVE	I/O	Special Engineering Test Pin; Include Pull-Down Resister. Reserve is “0”. (1: Enable; 0:Disable)
56	XIN	I	Crystal Oscillator Input
57	XOUT	O	Crystal Oscillator Output
58	V_{DDIO4}	P/I	Digital IO 3.3V Power Input Pin
59	MCLK	O	PCM System Clock Output
60	V_{SS7}	G	Digital IO Ground Pin
61	V_{DD5}	P/I	Digital Core 1.8V Power Input Pin
62	V_{SS8}	G	Digital Core Ground Pin
63	NC10	NC	No Connection, Include Pull-Down Resister, Reserve is “0”.
64	NC11	NC	No Connection, Include Pull-Down Resister, Reserve is “0”.

NOTE :

I: Input only

O: Output only

I/O: Input or Output

G: Ground

P: Power supply

AI : Analog Input

NC: No Connection

4.Architecture Detail:

4-1 DigIn/DigOut Interface:

Only master clock mode could be supported. The system clock (MCLK), word clock (WCLK), bit clock (BCLK) are outputs synchronously generated on-chip for audio ADC and DAC. The output SysClk/WordClk ratio and SysClk/BitClk ratio are both fixed value - 256 times and 64 times. The device accepts & output the left justified & I²S digital audio format & the set by the pin .16 & pin.17.

For an illustration of the require relationship between MCLK, BCLK and WCLK, see the figure as blew.

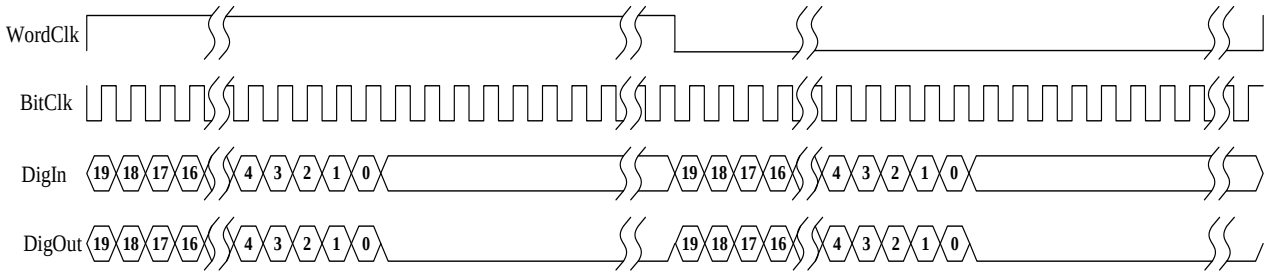


FIG. LJ DigIn/DigOut Format Timing

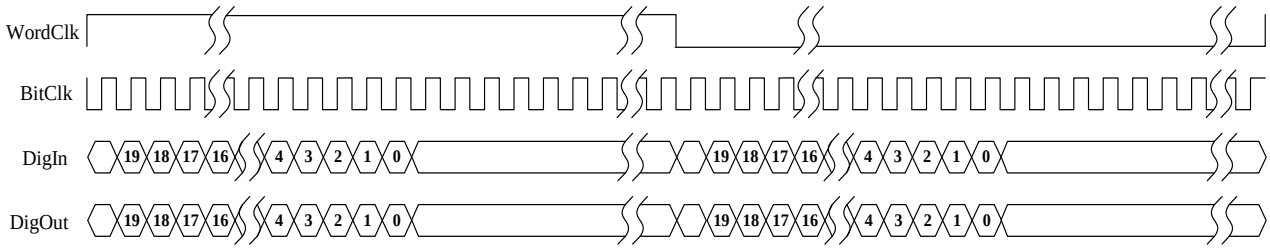


FIG. I²S DigIn/DigOut Format Timing

4-2 Fade Unit (Effect-ON / -OFF)

AT6861EM apply a fade unit to anti the noise when switch AT6861EM internal program or download external effect program. The fade will cost about 300ms. The Effect-ON when the FADE (Pin.53) is “0” and Effect-OFF when the FADE (Pin.53) is “1”.

4-3. Reset Circuitry:

The AT6861EM may be asynchronously reset using the /Reset pin, with a minimum pulse width of 163ns. This will start a Data RAM self test and initial to zero. After reset, the Data RAM will start self test and initial to zero, all internal counters and state registers set to zero.

4-4. Serial Microprocessor Interface:

The basic format for the micro serial interface is:

Attn Sel R/W A7 A6 A5 A4 A3 A2 A1 A0 DN DN-1 DN-2 … D2 D1 D0 Attn Desel

Attn : A 0-1-0 is used to signal attention/ start.

Sel / Desel : 0: Select; 1: Deselect.

A7 – A0 : Address.

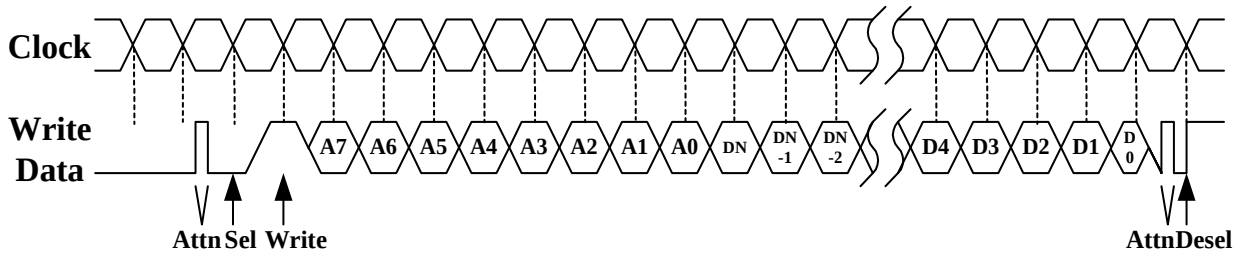
R /W : 0: Read; 1: Write.

DN – D0 : Data

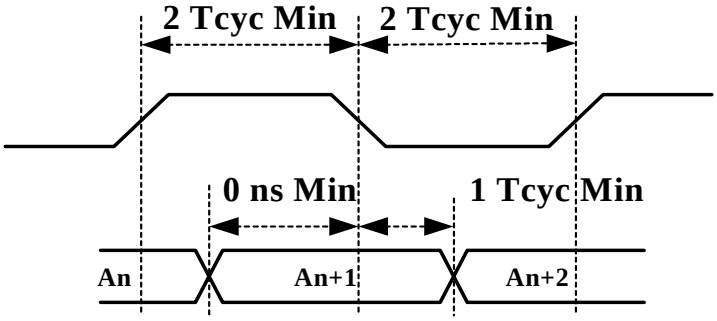
Attn Desel: Write mode only.

Note:

1. There is a short period of High- Z during a read between A0 and the first data bit shifted out. This period must be at least 5 system clocks long, 1 word clock long if not in direct mode (CS0 [3]).
2. As long as data is being sent during a write, the address will be automatically incremented. Therefore only a start address need be sent.
3. The phase of the clock is unimportant.



Write Timing (Tcyc = 1/FmasterClk)



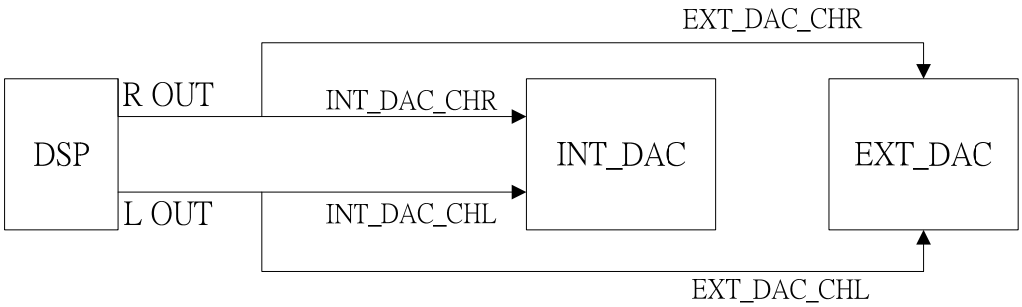
4-5 Internal Program List:

The 16 proven high-quality ROM programs are ready to go. By setting the chip to internal mode, the four program pins PROG [3:0] could be used to select the different algorithms. PROG[0] is SDA and PROG[1] is SCL pin.

PROG [3:0]	Name	Description
0000	Hall 1	Bright hall reverb for drums, guitars, and vocals.
0001	Hall 2	Warm hall for acoustic guitars, pianos, and vocals.
0011	Room 1	Hardwood studio for acoustic instruments.
0010	Room 2	Ambience for acoustic mixes and synth sounds.
0110	Room 3	Warm room for guitars and rhythm instruments.
0111	Plate 1	Classic plate reverb for lead vocals and instruments.
0101	Plate 2	Sizzling bright plate reverb for vocals and drums.
0100	Plate 3	Short vintage plate reverb for snares and guitars.
1100	Chorus	Stereo chorus for guitars and pianos.
1101	Flange	Stereo flanger for jet wash effects.
1111	Delay 1	125ms slapback delay for vocals and guitars.
1110	Delay 2	0.68sec slapback delay for vocals and guitars.
1010	Room/Chorus 1	Simulated a small space reverb add stereo chorus effect.
1011	Room/Chorus 2	The small space reverb is same with Room/Chorus1, but added more stereo chorus effect.
1001	Vocal Cancel	Removes lead vocals from many stereo recordings.
1000	Rotary Speaker	Rotary speaker emulation for organs and guitars.

4-6 Internal DAC & External DAC:

AT6861EM output digital data to Internal DAC & External DAC at the same time (L OUT = INT_DAC_CHL = EXT_DAC_CHL；R OUT = INT_DAC_CHR = EXT_DAC_CHR), so AT6861EM was only supported to output 2-channel digital data, see the figure as blew..



5. AC and DC Specification

5-1ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
VDDIO1, VDDIO2, VDDIO3, VDDIO4	3.0	3.6	V
VDDDAH1,VDDDAH2	3.0	3.6	V
VDD1,VDD2,VDD3,VDD4,VDD5,VDD6,VDD7	1.62	1.98	V
VDDDA	1.62	1.98	V
Storage temperature	-25	125	^{o}C
Ambient temperature with power applied	0	70	^{o}C

*Note: Stresses above those listed may cause permanent damage to the devices

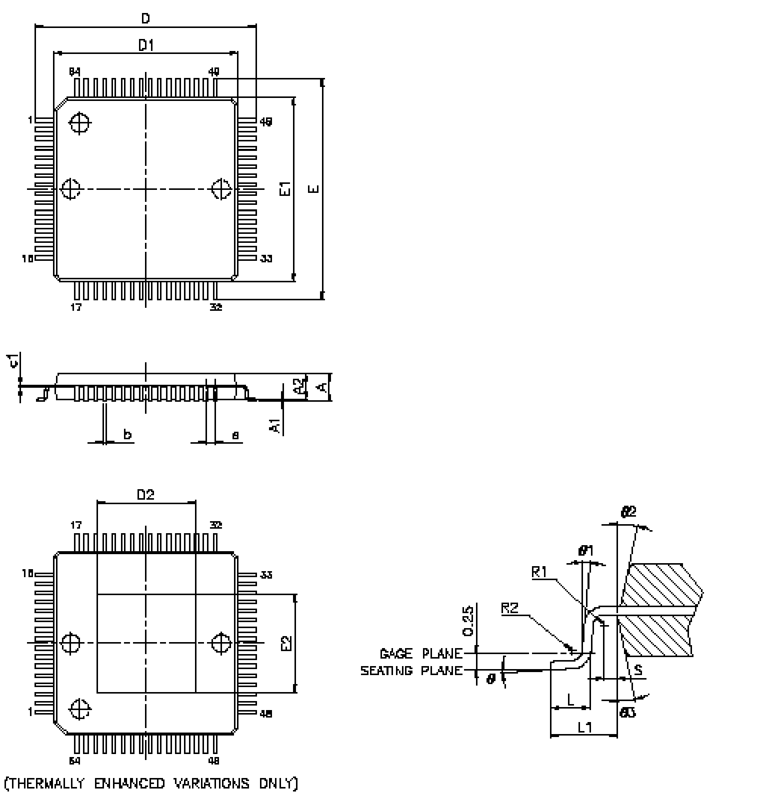
5-2D.C Characteristics (VDDIO=3.3V±10%, VDD=1.8V±10%Ta=0-70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.8	3.3		V
V_{IL}	Input Low Voltage			0	0.95	V
V_{OH}	Output High Voltage	I_{OH} = -8mA	3.15	V_{DDIO1}	--	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA	--	0	0.15	V
I_{IL}	Input Leakage Current	0V <V_{IN} < V_{DD}	--	54.5	--	μA
Z_{PH}	Pull High Resistor Impedance		--	55	--	Kohm
Z_{PL}	Pull Low Resistor Impedance		--	55.5	--	Kohm
$I_{DD,OPT}$	Operating Current	F_{OSC}= 12.288MHz	--	15.8	--	mA
$I_{LIMIT18}$	Pin.30 Load Current				85	mA
$I_{LIMIT33}$	Pin.29 Load Current				85	mA

Table. DC Electrical Characteristics

6. Package Information

LQFP64



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	–	0.16
D	11.75	12.00	12.25
D1	9.80	10.00	10.10
E	11.75	12.00	12.25
E1	9.80	10.00	10.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.18 REF		
R2	0.15 REF		

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
210X21E	4.27	5.33	4.27	5.33
260X26E	5.28	6.60	5.28	6.60

NOTES:

1. JEDEC OUTLINE :
   MS-026 BCD
   MS-026 BCD-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

TITLE: LOW PROFILE PLASTIC QUAD FLAT PACKAGE DATA SHEET 64 LEADS
J1-08064-001
APPD: Erik DATE: 7/11/07
FILE: J1-08064-001-08 REV: 08 SHT: 1