Product information presented is current as of publication date. Details are subject to change without notice.

INTEGRATED AMOLED POWERSOLUTION WITH ADJUSTABLE BOOST AND INVERTING CONVERTERS

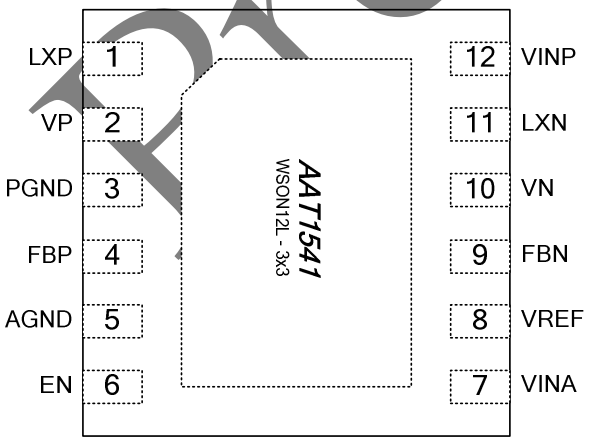
FEATURES

- **Integrated 1.5MHz Synchronous Boost & Inverting Regulators**
- **2.3V to 5.5V Input Voltage Range**
- **4.6V to 7V Adjustable True Shutdown Boost Output**
- **–5V to –1.5V Adjustable Inverting Output**
- **85% Typical Efficiency**
- **Integrated High Efficiency Light-Load Mode**
- **Output Current Up to 200mA**
- **<1μA Shutdown Current**
- **Over Current /Short Circuit Protection**
- **160°C Thermal Shutdown Protection**
- **WSON12L-3x3 Package Available**

APPLICATIONS

- **Active Matrix OLED**
- **Portable Multi-Media Devices**

PIN CONFIGURATION

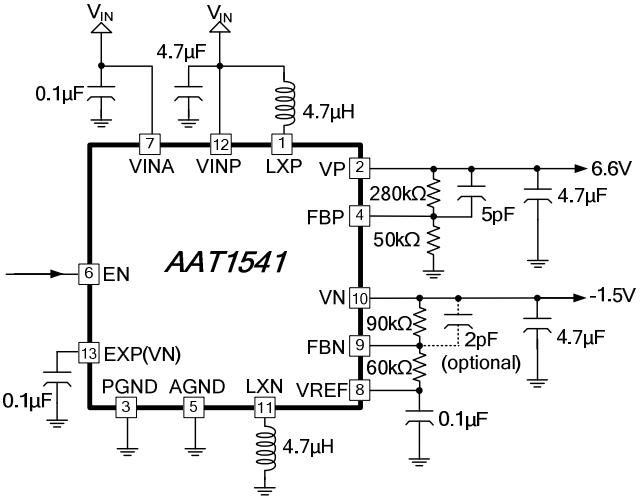


GENERAL DESCRIPTION

The AAT1541 is an integrated power solution tailored for AMOLED and mobile devices. It includes a Boost and an inverting switching regulator operating at 1.5MHz and for V_{IN} ranging from 2.3V to 5.5V. Output voltage of the Boost regulator can be adjusted from 4.6V to 7V through external feedback resistors, and the regulator is implemented with true-shutdown function to eliminate possible power loss during off mode. The inverting regulator output can also be adjusted from –5V to –1.5V. Both regulators are synchronous converters with internal compensation, thereby reducing external part count to minimal.

During light load operation, both converters enters light-load mode, reducing the quiescent current down to less than 1mA to elevate power efficiency, making AAT1541 ideal for mobile applications.

TYPICAL APPLICATION



ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1541	AAT1541-Q28-T	Q28: WSON12L-3x3	T: Tape and Reel	–40°C to +85°C	1541 XXXX XXXX	Part Name Lot No. (4~6 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	VALUE	UNIT
Power Supply Voltage (VINP, VINA)	V_{IN}	–0.3 to +7.0	V
Logic & Feedback Input Voltage (EN, FBN, FBP)	V_{CTL}	–0.3 to (V_{INP} +0.3)	V
Output Switch Current (VP, VN)	I_{LXP}, I_{LXN}	Internally Limited	A
Boost Regulator Switch Node Voltage (LXP)	V_{LXP}	–0.3 to (V_P +0.3)	V
Boost Output Voltage (VP)	VP	–0.3 to +10.0	V
Inverting Regulator Switch Node Voltage (LXN)	V_{LXN}	(V_N –0.3) to (V_{INP} +0.3)	V
Inverting Output Voltage (VN)	V_N	–7 to (PGND +0.3)	V
Power Dissipation, @ T_C = +25°C , T_J = +125°C	P_d	2.128	W
Junction Temperature	T_J	125	°C
Operating Temperature Range	T_C	–40 to +85	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Lead Temperature (Soldering 10 sec)	T_{SOLDER}	300	°C
ESD Protection (Human Body Mode)	V_{ESD}	2k	V

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Ambient Temperature	T_C	–40	+85	°C
Power Supply Voltage	V_{IN}	2.3	5.5	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_C = +25°C , unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{INP}, V_{INA}		2.3	-	5.5	V
UVLO VIN Rising Threshold Voltage	V_{UVLO}		-	2.2	-	V
UVLO Hysteresis	V_{HYST}		-	0.1	-	V
Supply Quiescent Current	I_{ON}	No Load: I_{VP} = I_{VN} = 0A	-	-	1	mA
	I_{SD}	V_{EN} = 0V	-	0.01	1.00	µA
Switching Frequency	f_{OSC}	PWM Mode	1.2	1.5	1.8	MHz
EN High Voltage Level	V_{ENH}	V_{INA} = V_{INP} = 2.3V to 4.5V	1.2	-	-	V
EN Low Voltage Level	V_{ENL}	V_{INA} = V_{INP} = 2.3V to 4.5V	-	-	0.4	V
EN Pull Low Resistance	R_{EN}		-	1	-	MΩ
Total System Efficiency	η_{LIGHT}	I_{VP} = I_{VN} = 10mA to 30mA; V_P = 6.6V; V_N = –1.5V	-	80	-	%
	η_{HEAVY}	I_{VP} = I_{VN} = 30mA to 150mA; V_P = 6.6V; V_N = –1.5V	-	85	-	%
Thermal Shutdown Temperature Threshold	T_{SD}		-	160	-	°C
Thermal Shutdown Temperature Hysteresis	T_{HYS}		-	10	-	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_C = +25°C , unless otherwise specified.)

Boost Converter

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Variation	VP	V_{INA} = V_{INP} = 2.5V to 4.5V, I_{VP} < 150mA, T_J = +25℃	–1	-	+1	%
		V_{INA} = V_{INP} = 3.7V, I_{VP} = 30mA, T_C = –40°C to +85°C	-	±0.6	-	%
Boost Channel Adjustable Range	VP		4.6	-	7.0	V
Power PMOS On Resistance	R_{DSON_P}		-	0.9	-	Ω
Power NMOS On Resistance	R_{DSON_N}		-	0.5	-	Ω
Inductor Peak Current Limit	I_{LX_MAX}		-	1.0	-	A
Maximum Load Current	I_{LOAD_MAX}	V_{INA} = V_{INP} = 2.9V to 4.5V	200	-	-	mA
Soft Start Period	t_{SS}		-	500	-	µs
Discharge Resistor	R_{DIS}		-	200	-	Ω
Light Load Mode Ripple	V_{RIP}	V_{INA} = V_{INP} = 2.9V to 4.5V, I_{VP} = 1mA, V_P = 6.6V	-	24	-	mV
GSM Line Transient Ripple	ΔVP_{GSM}	V_{INA} = V_{INP} = 3.2V to 3.7V, $T_{RISE / FALL}$ = 30µs, V_P = 6.6V I_{LOAD} = 50mA	-	30	-	mV

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_C = +25°C , unless otherwise specified.)

Inverting Converter

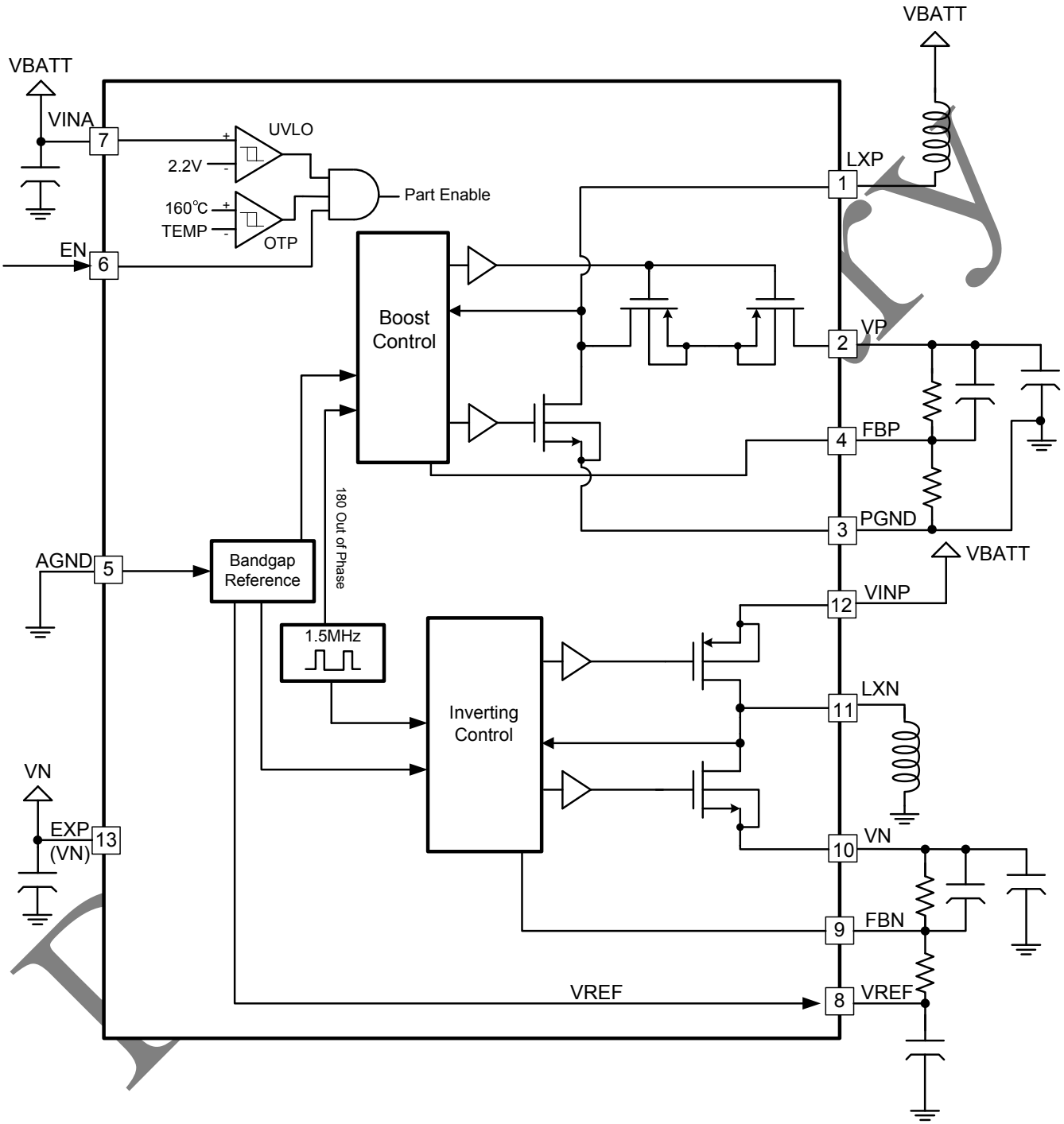
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Variation	V_N	V_{INA} = V_{INP} = 2.5V to 4.5V, I_{VN} < 150mA, T_J = +25°C	–1	-	+1	%
		V_{INA} = V_{INP} = 3.7V, I_{VN} = 30mA, T_C = –40°C to 85°C	-	±0.6	-	%
Inverting Channel Adjustable Range	V_N		–5.0	-	–1.5	V
Power PMOS On Resistance	R_{DSON_P}		-	0.9	-	Ω
Power NMOS On Resistance	R_{DSON_N}		-	0.5	-	Ω
Inductor Peak Current Limit	I_{LX_MAX}		-	1.0	-	A
Maximum Load Current	I_{LOAD_MAX}	V_{INA} = V_{INP} = 2.9V to 4.5V	200	-	-	mA
Soft Start Period	t_{SS}		-	500	-	µs
Discharge Resistor	R_{DIS}		-	300	-	Ω
Reference Voltage	V_{REF}	I_{VREF} = 10µA	0.988	1.000	1.012	V
Light Load Mode Ripple	V_{RIP}	V_{INA} = V_{INP} = 2.9V to 4.5V, I_{VN} = 1mA, V_N = –1.5V	-	18	-	mV
GSM Line Transient Ripple	ΔVN_{GSM}	V_{INA} = V_{INP} = 3.2V to 3.7V, $T_{RISE / FALL}$ = 30µs, V_N = –1.5V I_{LOAD} = 50mA	-	10	-	mV

Note 1. Performance for operation with VP < $V_{INP,A}$ + 0.4V is not guaranteed.

PIN DESCRIPTION

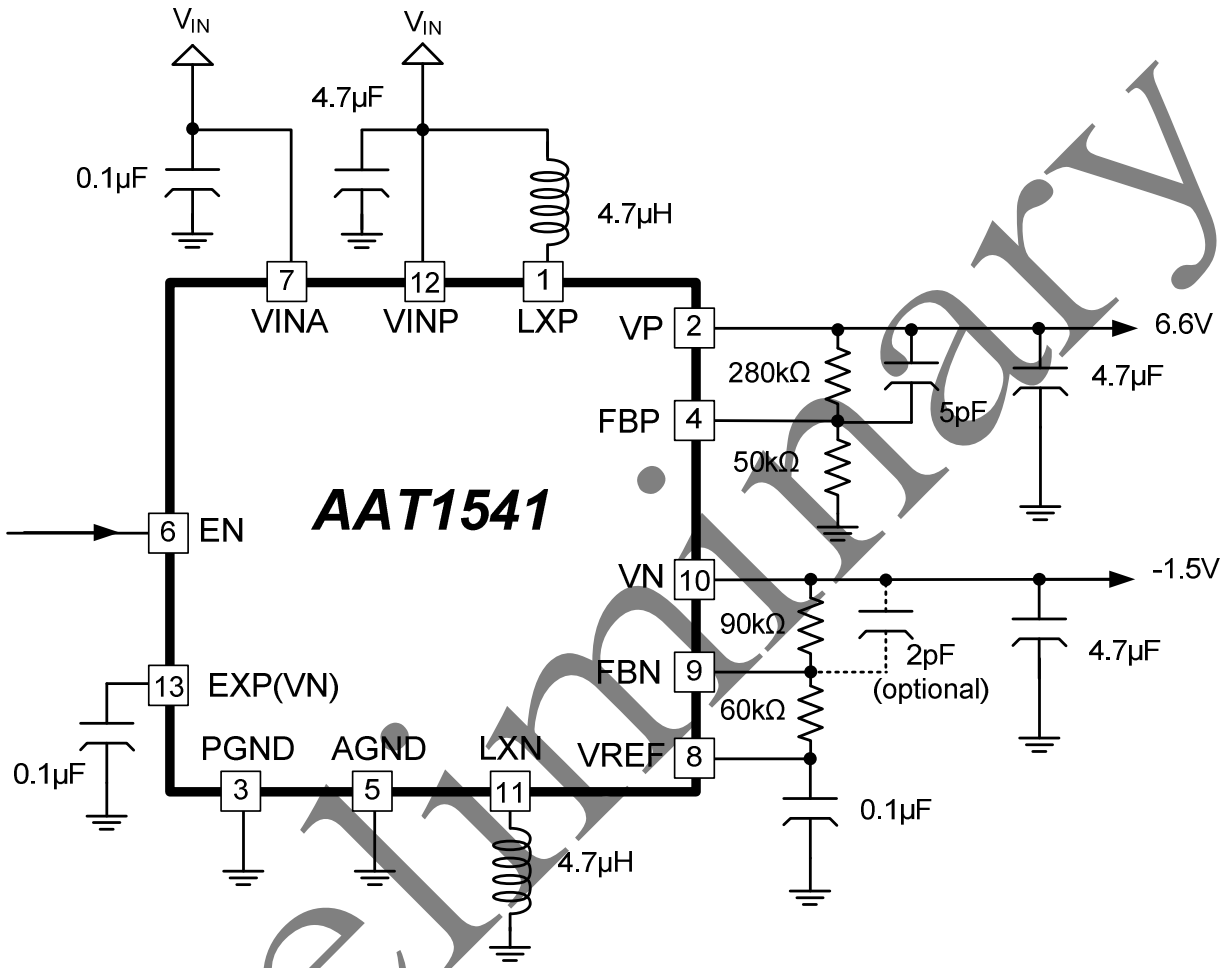
PIN	NAME	I/O	FUNCTION
1	LXP	I	Boost Regulator Switching Input Pin. LXP is connected to the drain terminals of the internal power MOSFETs. Connect this pin to battery or power supply through a 4.7µH (typ.) inductor.
2	VP	O	Boost Regulator Regulated Output Pin. Connect this pin to a 4.7µF (typ.) bypass capacitor to ground.
3	PGND	I	PWR Ground Pin: Connect this pin to ground through a low impedance trace.
4	FBP	I	Boost Regulator Feedback Pin: The boost regulator output voltage can be programmed with an external resistor network connected between this pin and the regulated output. The nominal voltage at this pin is at 1V when the output is regulated.
5	AGND	I	Analog Ground Pin: Connect this pin to a clean ground.
6	EN	I	Enable logic Input Pin: Pull the voltage at this pin above VENH to enable the device.
7	VINA	O	Analog Power Supply Input Pin: Connect this pin to a Li^+–Ion battery or an equivalent power source. Connecting VINA to ground through a close-by 0.1µF bypass capacitor is recommended.
8	VREF	O	Inverting Channel Reference Voltage Pin: Voltage at this pin is regulated at 1V when soft-start sequence is completed. This pin is used in the feedback network of the inverting channel.
9	FBN	I	Inverting Regulator Feedback Pin: The inverting regulator output voltage can be programmed with an external resistor feedback network connecting this pin, the regulated output, and the VREF Pin. The nominal voltage at this pin is at 0V when the output is regulated.
10	VN	O	Inverting Regulator Regulated Output Pin. Connect this pin to a 4.7µF (typ.) bypass capacitor to ground.
11	LXN	I	Inverting Regulator Switching Input Pin. LXN is connected to the drain terminals of the internal power MOSFETs. Connect this pin to ground through a 4.7µH (typ.) inductor.
12	VINP	I	Inverting Regulator Power Supply Input Pin: Connect this pin to a Li^+–Ion battery or an equivalent power source through a low impedance trace. Connecting VINP to ground through a 4.7µF bypass capacitor is recommended.
13	EXP(VN)	I	Exposed pad. Connect the pad to VN pin through a trace directly beneath the IC. A 0.1µH bypass capacitor connected between the EXP pad and ground is recommended.

FUNCTION BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT

AAT1541



DETAILED DESCRIPTION

The AAT1541 consists of highly efficient synchronous Boost and inverting regulators with current mode topology. Each channel of the AAT1541 includes a high-side PFET and a low-side NFET with low on-resistance to maximize efficiency and eliminate the need for an external Schottky diode.

Enable

The Enable (EN) pin allows user to enable and disable the converter for purposes such as power-up sequencing. With EN is pulled above 1.2V, the converter is enabled and the internal reference circuit wakes up. The AAT1541 then initiates soft start. When CNTRL is pulled below 0.4V, both converters are simultaneously disabled, and all MOSFET switches are turned off, while the output capacitors are discharged through internal resistors.

Soft-Start

The AAT1541 has a built-in soft-start mechanism to minimize the inrush current during start-up. Once the device is enabled, the step-up converter begins to charge its output capacitor with a constant slope. The soft start period for the step-up converter typically lasts 500µs, then the Inverting channel output starts to ramp down. The soft-start period for the inverting channel also lasts about 500µs. A typical output voltage waveform during soft-start is shown in Figure 1.

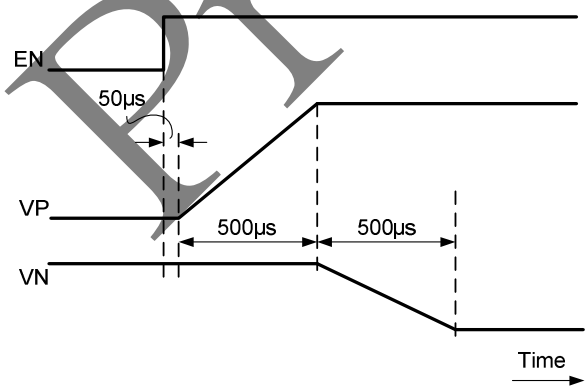


Figure 1. Soft-Start Waveform

PWM Mode Operation

AAT1541 adopt the peak current mode pulse width modulation (PWM) control scheme for fast transient response and cycle-by-cycle current limiting. The scheme maintains a constant frequency and varies the duty ratio according to the output voltage and load current. The PWM mode provides high efficiency at medium to heavy load conditions, and reduces output ripple. In this operating mode, a first power MOSFET (NMOS for step-up and PMOS for inverting) turns on each cycle for at least a self-adjusted minimum on-time to raise the inductor current, and turns off when the sawtooth signal reaches the error amplifier output (EO). The sawtooth signal is composed of the sensed inductor current and an artificial slope compensation ramp. After the first power MOSFET is turned off, a second power MOSFET (PMOS for step-up and NMOS for inverting) is turned on until reverse current is detected or when the next cycle begins. The detection of reverse current ensures inductor current always flows in the direction that forces the output voltage away from the GND, thereby preventing waste of energy and raising regulator efficiency.

Light Load Mode Operation

The AAT1541 is implemented with a highly efficient light load operation mode, which is activated during very light load condition, typically at load current below 10mA (varies with V_{IN} and V_{OUT}). In a light load condition, the system is only awake temporarily to charge the output and maintain its level around the nominal value, while most circuits are usually turned-off to conserve energy. A precision comparator sets the system sleep/wake-up thresholds, and controls the output ripple typically below 0.5% of the nominal value.

Under Voltage Lock Out (UVLO)

The AAT1541 protects the devices from malfunctioning due to low supply voltage by preventing the internal circuitry from turning-on when the supply voltage at the VIN pin is below 2.2V. Once the device is turned-on, a built-in 100mV hysteresis automatically adjusts the UVLO threshold so the circuit turns off the whole device once VIN voltage drops below 2.1V. The internal power MOSFETs are switched off during the UVLO state.

Thermal Shut Down

The AAT1541 is implemented with a thermal protection function, which turns off the device when the internal temperature of the system is too high. The thermal shutdown rising threshold temperature is 160°C (typ.) with a 15°C (typ.) hysteresis.

Short Circuit Protection (SCP)

When the inductor current of any channel exceeds the current limit of 1A (typ.), the internal power MOSFETs switch states to lower the inductor current, thus the peak current is clamped at 1A for over-current protection (OCP). If the load continues to draw a large current and the output voltage drops below (or rises above for the inverting channel) 60% of the nominal value for over 50ms (typ.), the SCP state is flagged and system will shutdown automatically. Once the SCP function is triggered, the device can be re-started by resetting EN pin low and high again.

DESIGN PROCEDURE

Inductor Selection

For optimal operation, 4.7µH inductors are recommended for both step-up and inverting channels, the current rating of the inductors should be safely above (1.5X) the inductor maximum peak current (I_{PMAX}), which can be approximated by:

$$I_{PMAX} = \frac{I_{LMAX}}{D'_{MIN}} + 0.2$$

$$\text{Step-up channel: } D'_{MIN} = 1 - \frac{1.2 \times V_{OUT} - V_{IN\_MIN}}{1.2 \times V_{OUT}}$$

$$\text{Inverting channel: } D'_{MIN} = 1 - \frac{1.2 \times V_{OUT}}{1.2 \times V_{OUT} - V_{IN\_MIN}}$$

ILMAX: maximum load current
VIN_MIN: minimum input voltage
Note: VOUT is negative for the inverting channel

Input and Output Capacitor Selection

For optimal operation, low ESR ceramic capacitors are recommended to be placed close to the VINP and VINA pins. Typically a 4.7µF capacitor for VINP and a 0.1µF capacitor for VINA would be sufficient for normal operation. For both channels, the typical value of output capacitors is 4.7µF or larger to maintain output stability. If small output ripple in the light load mode is critical for the application, 10µF capacitors are recommended for both channels. In PWM mode operation, output voltage ripples are mostly caused by parasitic ESR, and choosing low ESR ceramic capacitors shall minimize the ripple in PWM mode for both channels.

Output Voltage Programming

The regulated output voltages at VP and VN are decided by external resistor networks. For the boost channel, the feedback pin voltage (V_{FBP}) is regulated at 1V, so the boost output voltage VP can be expressed by:

$$VP = \frac{RT_P + RB_P}{RB_P} \times 1V$$

Where RPT, RPB are illustrated in Figure 2.

The inverting channel feedback pin voltage (V_{FBN}) is regulated at 0V, while the VREF pin is kept at 1V, thus the inverting output voltage VN is expressed by:

$$VN = -\frac{RT_N}{RB_N} \times 1V$$

Where RNT, RNB are also shown in the figure below.

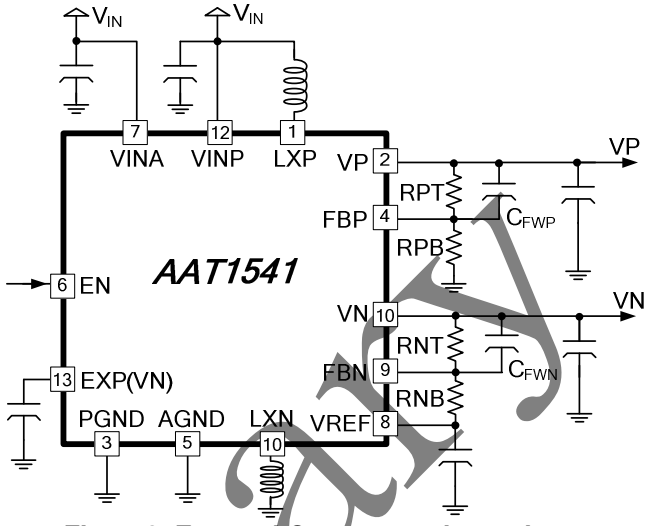


Figure2. External Component lustration

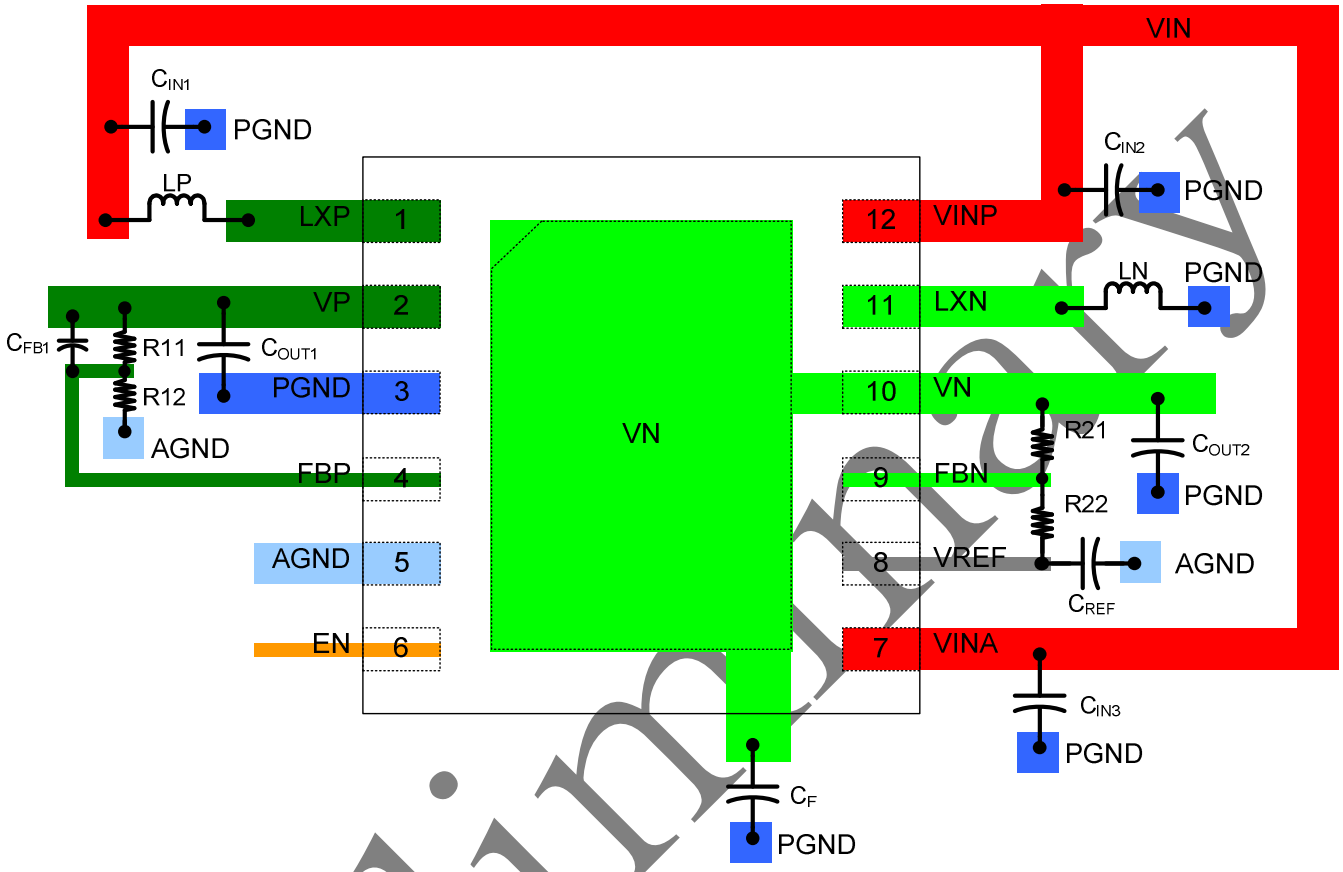
Compensation Information

The parasitic capacitance at the FB (FBP/FBN) pin forms a pole with the external voltage divider resistors. Feedfoward capacitors (C_{FWX}) is recommended to cancel out this pole. The value of C_{FWX} can be determined by:

$$C_{FW} = \frac{C_{PARASITIC} \times (RT_X // RB_X)}{RT_X - (RT_X // RB_X)}$$

Where $C_{PARASITIC}$ = 20pF (typ.). The feed-forward capacitor for the inverting channel (C_{FWN}) may often be unnecessary.

LAYOUT CONSIDERATIONS

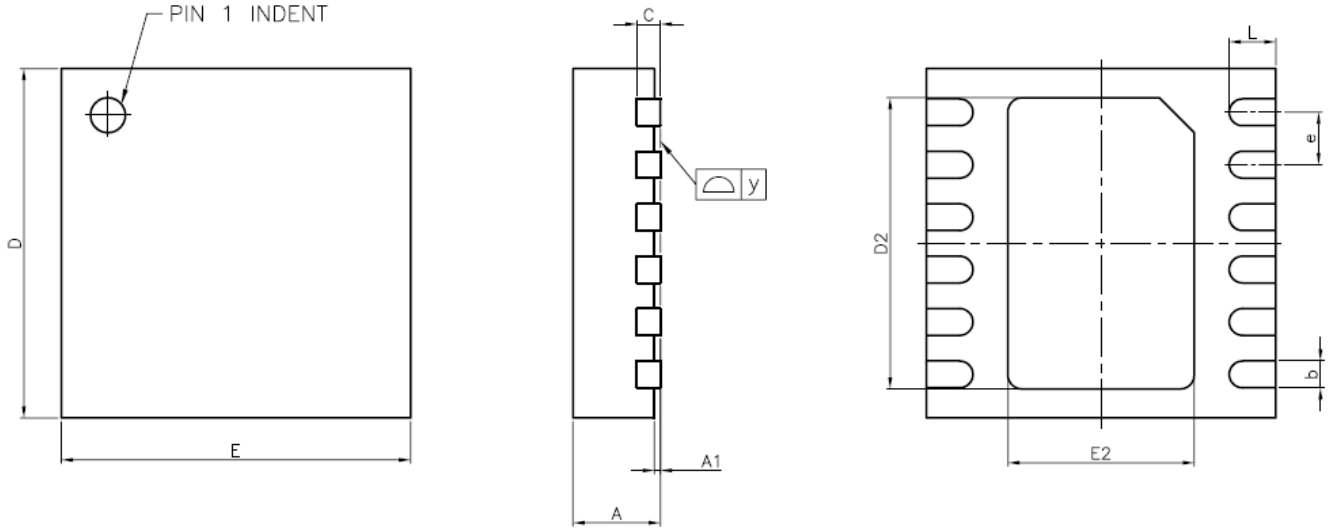


Layout Notice:

1. C_{IN1} / C_{IN2} / C_{IN3} should be placed near LP/ VINP/ VINA.
2. C_{OUT1} / C_{OUT2} / C_{REF} / C_F should be placed near AAT1541.
3. Inductors should be placed near LP and LN and keep sensitive component away from these traces.

PACKAGE DIMENSION

WSON12L-3x3



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.23	0.28
C	-----	0.20 REF.	-----
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.55	1.60	1.65
e	-----	0.45	-----
L	0.35	0.40	0.45
y	0.00	-----	0.075