MULTI-CHANNEL POWER SUPPLY FOR TFT LCD PANELS

BOOST, BUCK, CHARGE PUMPS, GPM, OP AMP, GAMMA REFERENCE, RESET

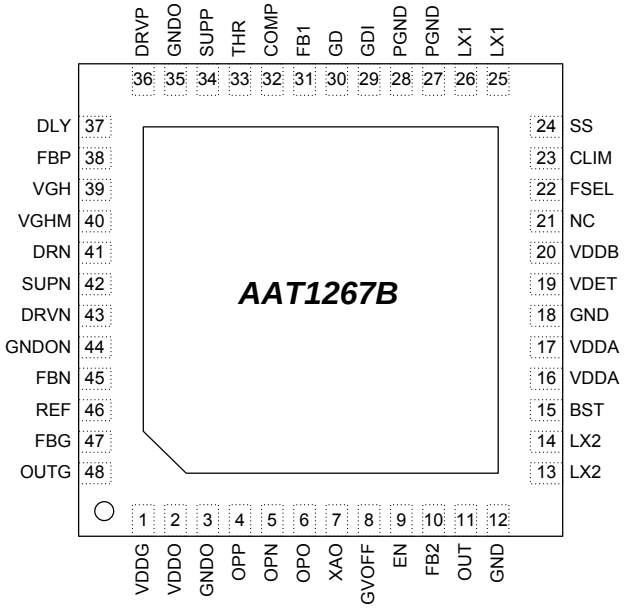
FEATURES

- 8V to 14V Input Supply Voltage Range
- 500kHz/750kHz Selectable Frequency
- Current Mode Boost Regulator
  - Built-In 20V, 3.6A, 0.1Ω N-MOSFET
  - Fast Load Transient Response
  - Adjustable Soft-Start
  - Adjustable Current Limit
  - External PMOS Gate Control for AVDD Sequencing
- Current Mode Buck Regulator
  - Built-in 16.5V, 3.2A, 0.1Ω, MOSFET
  - Fast Load Transition Response
  - Internal Soft-Start and Compensation
- Positive Charge Pump Regulator
- Negative Charge Pump Regulator
- High Voltage Switch with Gate Pulse Modulation
  - Adjustable Power On Delay Time
- Operational Amplifier for VCOM Buffer
  - ±200mA Short-Circuit Current
  - 45V/μs Slew Rate
- High Accuracy LDO for Gamma Reference
  - ±1% Adjustable Output Voltage
  - Up to 60mA Load Current
- $\overline{\text{RESET}}$ (XAO Voltage Detector)
  - Adjustable Detecting Voltage
  - N-Channel Open-Drain Output
- Protection
  - Input Under-Voltage Lockout (UVLO)
  - Overload Current Protection (OCP)
  - Over Voltage Protection (OVP)
  - Short Circuit Protection (SCP)
  - Under Voltage Protection (UVP)
  - Thermal Shutdown (OTP)
- WQFN 48-7x7x0.75 Package

APPLICATIONS

- LCD TV Panel

PIN CONFIGURATION



GENERAL DESCRIPTION

The AAT1267B offers a compact power supply solution to provide all voltages required by a thin-film-transistor (TFT) liquid-crystal display (LCD) panel for TV applications running from a 12V supply rail. It includes a boost and a buck regulator, a positive and a negative regulated charge-pump, a high voltage switch with gate pulse modulation, an operational amplifier, a high accuracy LDO for gamma reference and one open drain $\overline{\text{RESET}}$ output.

The current mode boost regulator provides a fast transient response supply voltage for the source drivers. It provides an output voltage up to 20V from input voltages ranging from 8V to 14V. The boost regulator integrates a low R_{DSON} (0.1Ω) N-MOSFET, and operates at a selectable switching frequency of either 500kHz or 750kHz, thereby minimizing board space while providing good efficiency. An externally programmed soft start minimizes inrush current and output overshoot. In addition, the AAT1267B integrates a control block that can drive an external P-Channel MOSFET to sequence power to source drivers.

The current mode buck regulator operates at either 500kHz or 750kHz and typically supplies system logic power (T-CON). It provides fast load transient response to pulsed loads while producing efficiencies over 90%. This buck regulator integrates a 16.5V, 3.2A, 0.1Ω, power MOSFET that allows the use of ultra-small inductors and ceramic capacitors. A built-in 7-bit digital soft-start function controls startup inrush currents.

The positive and negative charge pump regulators provide supply voltages for the TFT LCD's gate drivers. Both output voltages can be adjusted with external resistive voltage dividers. For improving TFT LCD image quality, a gate pulse modulation (GPM) circuit shapes the gate-on signal. The slope of the gate-on voltage and GPM power on delay time can be set by external resistor and capacitor.

The operational amplifier drives the LCD backplane (VCOM). This unity-gain buffer is capable of rail-to-rail input and output, ±200mA output short-circuit current, and a 45V/μs slew rate.

A high accuracy low dropout linear regulator is used as an adjustable reference voltage for gamma correction. The LDO guarantees a minimum 60mA output current, and has an internal high accuracy reference of +/-0.5%. The LDO output is set via external feedback resistors.

The $\overline{\text{RESET}}$ function is used to monitor the device supply voltage. A reset signal is issued via an open drain NMOS when the supply is below a programmable threshold. The threshold is set by external resistors and the delay time is set by an external capacitor.

The AAT1267B device includes various protection features such as UVLO, OCP, OVP, SCP, UVP and thermal shutdown.

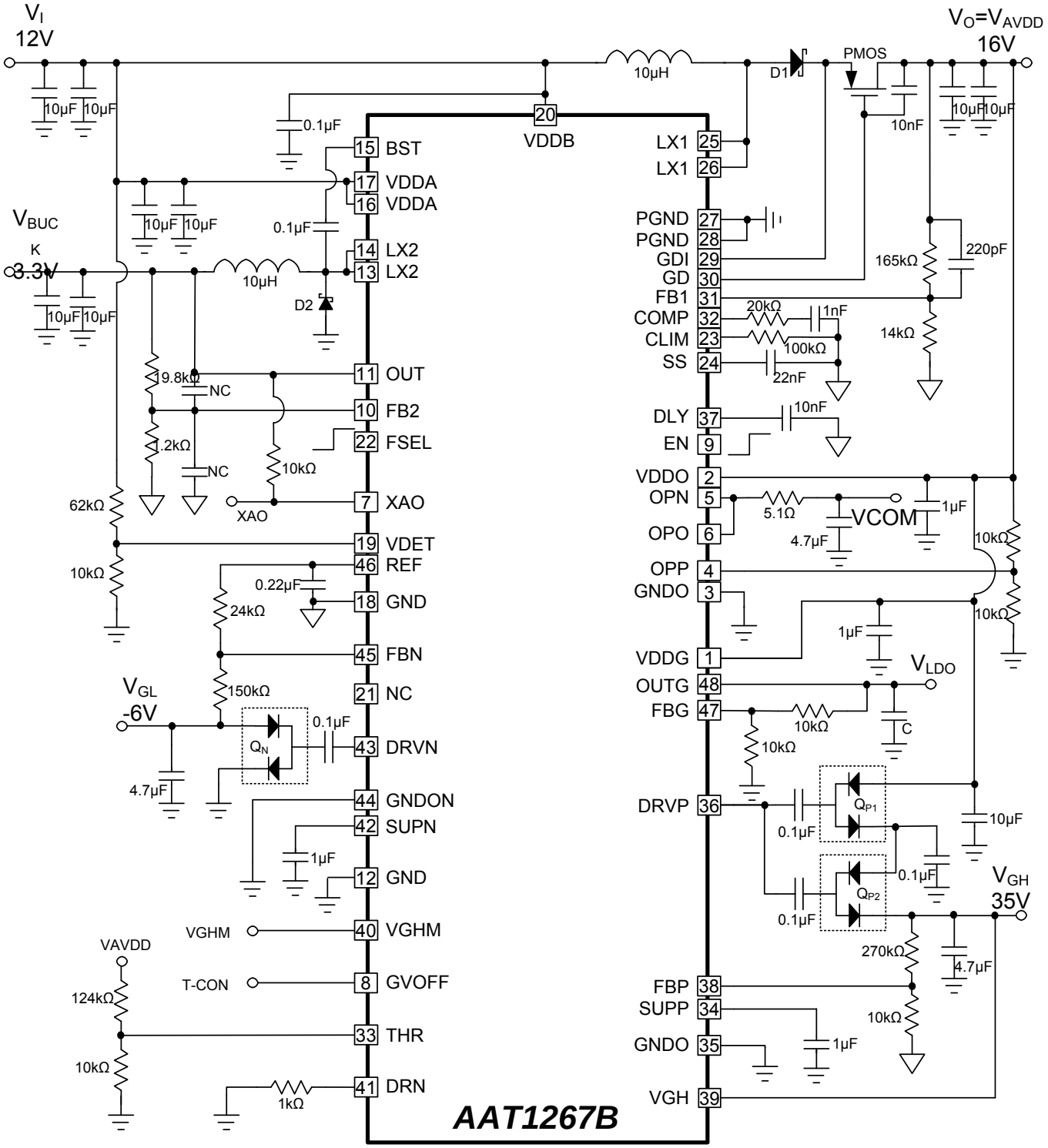
The AAT1267B is available in a small 7x7x0.75mm, ultra-thin, 48 pin QFN package with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40°C to +85°C ambient temperature range.

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1267B	AAT1267B-Q51-T	Q51:WQFN 48-7*7	T: Tape and Reel	–40°C to +85°C	AAT1267B XXXXXX XXXX	Device Type Lot no. (6~9 Digits) Date Code. (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VDDA, VDDB, SUPN, EN, FSEL to GND	V_{IN}	–0.3 to +16.5	V
PGND, GNDO, GNDON to GND	V_{IN}	–0.3 to +0.3	V
SUPP, GDI, GD, VDDO, OPP, OPN, VDDG, BST to GND	V_{H1}	–0.3 to +20	V
LX1 to PGND	V_{H2}	–0.3 to +20	V
LX2 to GND	V_{H3}	–0.3 to (V_{IN}+0.3)	V
VGHM, VGH, DRN to GND	V_{H4}	–0.3 to +40.0	V
VGH to VGHM	V_{H5}	–0.3 to +40.0	V
VGH, VGHM to DRN	V_{H6}	–0.3 to +40.0	V
FB1, FB2, FBP, FBN, XAO, VDET, GVOFF, CLIM, SS, COMP, THR, DLY1, REF, FBG, OUT to GND	V_{I1}	–0.3 to +6.5	V
Output Voltage1 (DRVP to GNDO)	V_{O1}	–0.3 to (V_{H1} +0.3)	V
Output Voltage2 (DRVN to GNDON)	V_{O2}	–0.3 to (V_{IN} +0.3)	V
Output Voltage3 (OPO to GNDO)	V_{O3}	–0.3 to (V_{H1} +0.3)	V
Output Voltage4 (OUTG to GND)	V_{O4}	–0.3 to (V_{H1} +0.3)	V
Operating Ambient Temperature Range	T_C	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Range	θ_{JA}	29	°C
Power Dissipation @ T_C = +25°C , T_J = +125°C	P_d	3.448	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DDA} = V_{DDB} = 12V, T_C = +25°C , unless otherwise specified.)

General

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDDA, VDDB Input Voltage Range	V_{DD}		8	12	14	V
VDDA, VDDB Quiescent Current	I_Q	LX not Switching	-	5	-	mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	6	7	8	V
		V_{IN} Falling Hysteresis	0.1	0.3	0.5	V
Switching Frequency	f_{OSC}	FSEL = V_{IN}	630	750	870	kHz
		FSEL = GND	420	500	580	kHz
Thermal Shutdown Threshold	T_{SHDN}	Falling Edge	-	160	-	°C

Boost Regulator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range	-		V_{IN}	-	18	V
FB1 Regulation Voltage	V_{FB1}		1.2375	1.2500	1.2625	V
FB1 Input Leakage Current	I_{Leak1}	V_{FB1} = 1.25v	–40	0	+40	nA
FB1 Line Regulation	-	10.8V< V_{IN} <13.2V	-	0.08	-	%V
FB1 Load Regulation	-	0< I_{LOAD} < Full	-	0.5	-	%
LX1 Current Limit	I_{LIM1}	R_{CLIM} > 50kΩ or Floating	3.0	3.6	-	A
LX1 ON-Resistance	R_{ON_LX1}		-	150	300	mΩ
LX1 Leakage Current	I_{Leak2}		-	0.01	5.00	μA
Maximum Duty Cycle	-		70	80	85	%
FB1 SCP Trip Level	V_{S1}	Falling Edge	0.45	0.50	0.55	V
FB1 UVP Level	V_{F1}	Falling Edge	0.96	1.00	1.04	V
Duration to Trigger UVP Condition	t_{F1}		-	50	-	ms
Internal Soft-Start Time	t_{SS1}	C_{SS} < 220pf	-	16	-	ms
SS Charge Current	I_{SS}	C_{SS} > 220pf	4	5	6	μA
Transconductance	g_m		70	105	240	μS
Voltage Gain	A_V		-	1,400	-	V/V

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DDA} = V_{DDB} = 12V, T_C = +25°C , unless otherwise specified.)

Buck Regulator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range	-		1.5	-	5.0	V
OUT Voltage in Fixed Mode	V_{FB33}	FB2 = GND	3.267	3.300	3.333	V
FB2 Voltage in Adjustable Mode	V_{FB2}		1.2375	1.2500	1.2625	V
FB2 Input Leakage Current	I_{Leak3}		–40	0	+40	nA
FB2 Line Regulation	-	10.8V< V_{IN} <13.2V	-	0.1	-	%/V
FB2 Load Regulation	-	0 < I_{LOAD} < 2A	-	0.5	-	%/A
LX2 Current Limit	I_{LIM2}		2.5	3.2	-	A
LX2 to VDDA NMOS Switch ON-Resistance	R_{ON_LX2}		-	100	200	mΩ
Maximum Duty Cycle	-		70	80	85	%
FB2 SCP Trip Level	V_{S2}	Falling Edge	0.45	0.5	0.55	V
FB2 UVP Trip Level	V_{F2}	Falling Edge	0.96	1.00	1.04	V
Duration to Trigger UVP Condition	t_{F2}		-	50	-	ms
Internal Soft-Start Time	t_{SS2}		-	3	-	ms

Positive Charge Pump Regulator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
FBP Regulation Voltage	V_{FBP}		1.225	1.250	1.275	V
FBP Input Leakage Current	I_{Leak4}	V_{FBP} = 1.25V	–40	0	+40	nA
FBP Line Regulation Error	-	10.8V< V_{IN} <13.2V	-	-	6	mV
DRVN P-MOSFET ON-Resistance	R_{ON_P3}		-	4	-	Ω
DRVP N-MOSFET ON-Resistance	R_{ON_N3}		-	1	-	Ω
FBP SCP Trip Level	V_{S3}	Falling Edge	0.45	0.50	0.55	V
FBP UVP Trip Level	V_{F3}	Falling Edge	0.96	1.00	1.04	V
Duration to Trigger Fault Condition	t_{F3}		-	50	-	ms
Internal Soft-Start Time	t_{SS3}		-	3	-	ms

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DDA} = V_{DDB} = 12V, T_C = +25°C , unless otherwise specified.)

Negative Charge Pump Regulator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
FBN Regulation Voltage	V_{FBN}		0.21	0.25	0.29	V
FBN Input Leakage Current	I_{Leak5}	V_{FBN} = 0.25V	–40	0	+40	nA
FBN Line Regulation Error	-	10.8V< V_{IN} <13.2V	-	-	6	mV
DRVN P-MOSFET ON-Resistance	R_{ON_P4}		-	4	-	Ω
DRVN N-MOSFET ON-Resistance	R_{ON_N4}		-	1	-	Ω
FBN SCP Trip Level	V_{S4}	Falling Edge	0.80	0.85	0.90	V
FBN UVP Trip Level	V_{F4}	Falling Edge	0.40	0.45	0.50	V
Duration to Trigger Fault Condition	t_{F4}		-	50	-	ms
Internal Soft-Start Time	t_{SS4}		-	3	-	ms

High Voltage Switch with Gate Pulse Modulation

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
GVOFF Input Low Voltage	V_{IH}		-	-	0.6	V
GVOFF Input High Voltage	V_{IL}		1.5	-	5.5	V
GVOFF Input Current	I_{Leak6}		–40	0	+40	nA
GVOFF to VGHM Rising Propagation Delay	t_{RP}		-	100	-	ns
GVOFF to VGHM Falling Propagation Delay	t_{FP}		-	250	-	ns
VGH Input Voltage Range	V_{IGH}		-	-	40	V
VGHM to VGH Switch On-Resistance	R_{ON_P5}		-	5	10	Ω
VGHM to DRN Switch On-Resistance	R_{ON_P6}		-	40	60	Ω
THR to VGHM Voltage Gain			-	10	-	V/V
DLY Charge Current	I_{DLY}		5	7	9	μA

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DDA} = V_{DDB} = 12V, T_C = +25°C , unless otherwise specified.)

Operational Amplifier for VCOM Buffer

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDDO Input Voltage Range	V_{OPI}		8	-	18	V
VDDO Supply Current	I_{OP}		-	1.5	-	mA
Input Offset Voltage	V_{OS}		-	-	20	mV
Output Voltage Swing High	V_{OH}	I_{OPO} = 10mA	VDDO –300	VDDO –100	-	mV
Output Voltage Swing Low	V_{OL}	I_{OPO} = –10mA	-	VDDO +100	VDDO +300	mV
Short Circuit Current	I_{SHORT}	OPO = OPN, OPP = 1/2 * V_{AVDD}	-	±200	-	mA
–3dB Bandwidth	f_{-3dB}	R_L = 10kΩ, C_L = 10pF	-	20	-	MHz
Slew Rate	SR		-	45	-	V/µs

High Accuracy LDO for Gamma Reference

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDDG Input Voltage Range	V_{OPI}		10	-	18	V
Quiescent Current	I_Q		-	125	250	µA
FBG Feedback Voltage	V_{FBG}		1.2375	1.2500	1.2625	V
FBG Input Leakage Current	I_{Leak7}	V_{FBG} = 1.25V	–40	0	+40	nA
Output Current Limit	I_{LIM3}		60	-	-	mA
Dropout Voltage	V_{DROP}	I_{LOAD} = 60mA	-	0.5	-	V

$\overline{\text{RESET}}$ (XAO Voltage Detector)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDET Detecting Voltage	V_{DET}	Falling Edge	1.2375	1.2500	1.2625	V
VDET Input Leakage Current	I_{Leak8}	V_{DET} = 1.25V	–40	0	+40	nA
XAO Output Voltage	V_{XAO}	V_{DET} = GND	-	-	0.4	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DDA} = V_{DDB} = 12V, T_C = +25°C , unless otherwise specified.)

Reference

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Output Voltage	V_{REF}	No External Load	1.2375	1.2500	1.2625	V
Reference Load Regulation	-	0 < I_{REF} < 50μA	-	-	5	mV
Reference Sink Current	I_{REF}	REF in Regulation	10	-	-	μA

Sequence Control

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
GD Output Sink Current	I_{GD}	EN = High, VGDI = V_{IN}	-	10	-	μA
GD ON Voltage	V_{GD}	EN = High, VGDI = V_{IN}	-	V_{IN} –5	-	V
EN Input High Voltage	V_{ENH}		1.5	-	V_{IN}	V
EN Input Low Voltage	V_{ENL}		-	-	0.6	V
EN Pull-Down Resistance	R_{EN}		-	1	-	MΩ

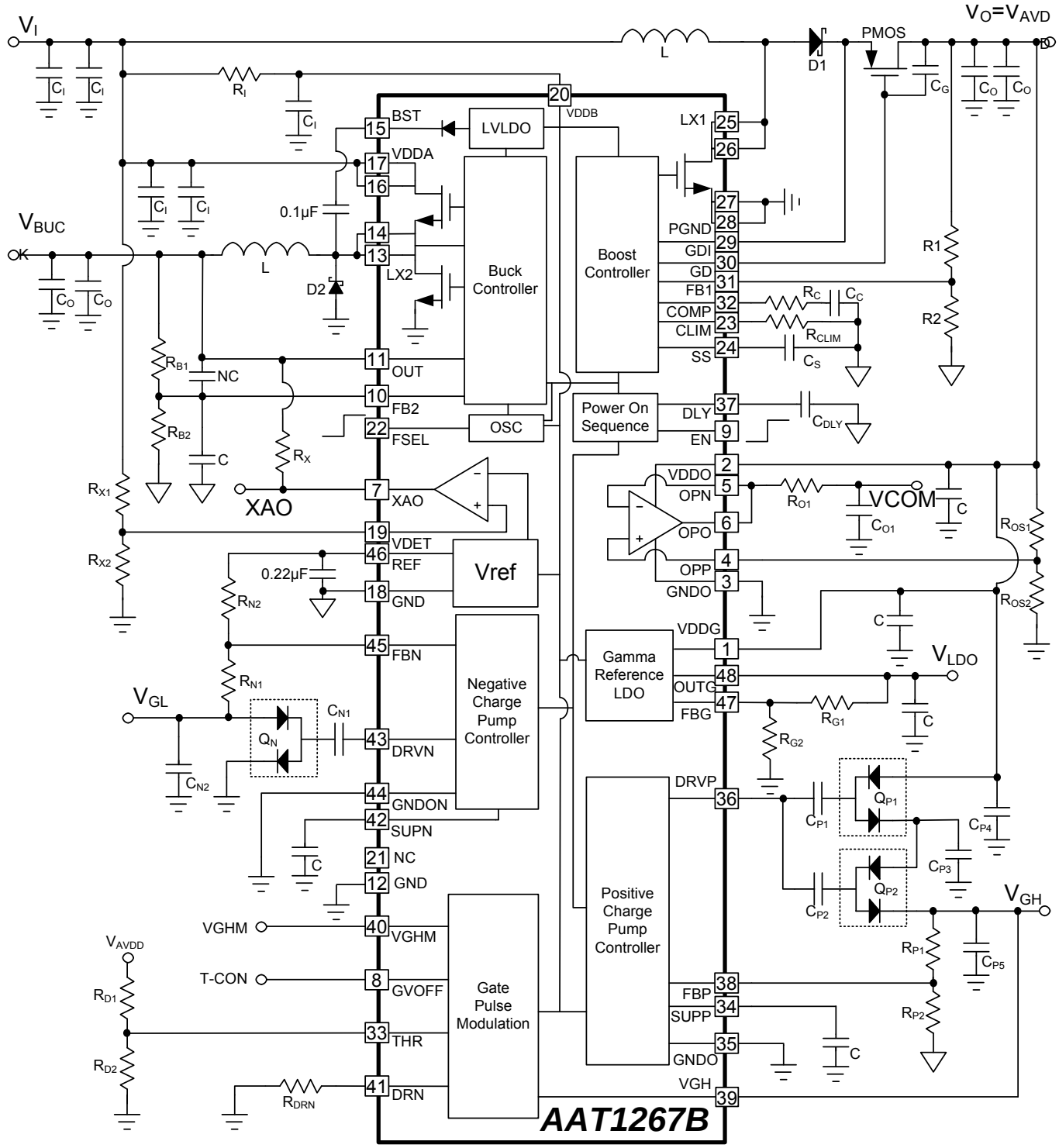
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	VDDG	I	Gamma Reference LDO Power Supply Input
2	VDDO	I	Operational Amplifier Power Supply Input
3	GNDO	-	Operational Amplifier Power Ground
4	OPP	I	Operational Amplifier Inverting Input
5	OPN	I	Operational Amplifier Non-inverting Input
6	OPO	O	Operational Amplifier Output
7	XAO	O	$\overline{\text{RESET}}$ Function Output
8	GVOFF	I	High Voltage Switch with Gate Pulse Modulation Logic Control Input
9	EN	I	Enable Input
10	FB2	I	Buck Regulator Feedback Input
11	OUT	O	Buck Regulator Output Sense Pin
12	GND	-	Analog GND
13	LX2	O	Buck Regulator Switching Node
14	LX2	O	Buck Regulator Switching Node
15	BST	I	Buck Regulator Bootstrap Capacitor Connection
16	VDDA	I	Buck Regulator Power Supply Input
17	VDDA	I	Buck Regulator Power Supply Input
18	GND	-	Analog GND
19	VDET	I	Voltage Detection Input ($\overline{\text{RESET}}$ Function)
20	VDDB	I	Internal 5V Linear Regulator and Startup Circuitry Power Supply Input
21	NC	-	Not Connected
22	FSEL	I	Frequency Select Pin
23	CLIM	I	Adjustable Boost Current Limit Pin
24	SS	I	Soft-Start Time Setting Pin
25	LX1	O	Boost Regulator Switching Node
26	LX1	O	Boost Regulator Switching Node
27	PGND	-	Boost Regulator Power Ground

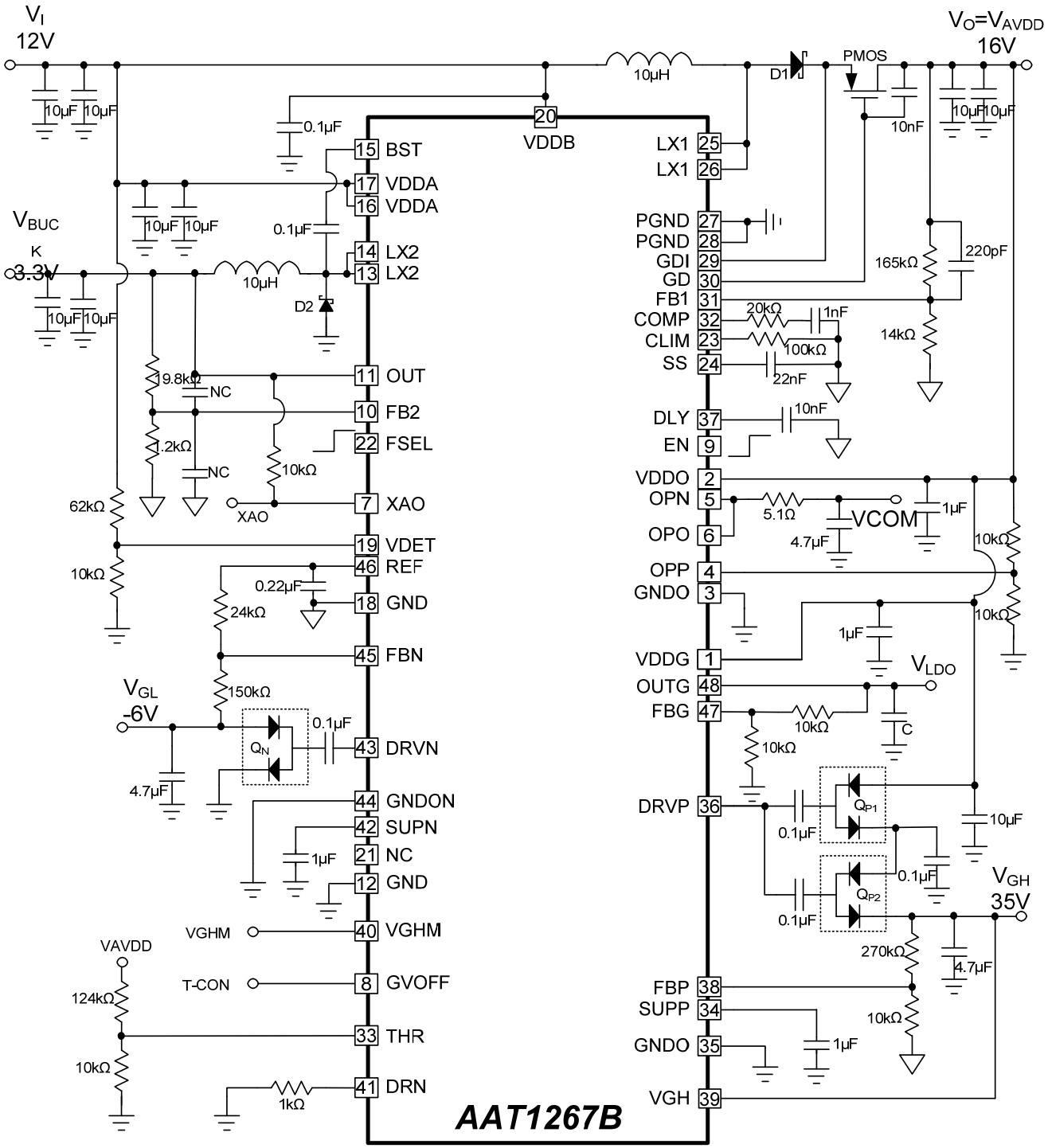
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
28	PGND	-	Boost Regulator Power Ground
29	GDI	I	Boost Regulator Output Sense Pin
30	GD	O	External PMOS Gate Control for Boost Regulator Sequencing
31	FB1	I	Boost Regulator Feedback Input
32	COMP	I	Boost Regulator Compensation Pin
33	THR	I	VGHM Falling Regulation Setting Pin
34	SUPP	I	Positive Charge Pump Regulator Power Supply Input
35	GNDO		VGH Charge Pump Ground
36	DRVP	O	VGH Charge Pump Regulator Output
37	DLY	I	High Voltage Switch with Gate Pulse Modulation (GPM) Delay Time Setting Pin
38	FBP	I	VGH Charge-Pump Regulator Feedback Input
39	VGH	I	High Voltage Switch with GPM Power Supply Input
40	VGHM	O	High Voltage Switch with GPM Output
41	DRN	O	High Voltage Switch with GPM Discharge Setting pin
42	SUPN	I	Negative Charge Pump Regulator Power Supply Input
43	DRVN	O	Negative Charge Pump Regulator Output
44	GNDON		VGL Charge Pump Ground
45	FBN	I	Negative Charge Pump Regulator Feedback Input
46	REF	O	Reference Output
47	FBG	I	Gamma Reference LDO Feedback Input
48	OUTG	O	Gamma Reference LDO Output
49	EP		Exposed PAD

FUNCTION BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



THEORY OF OPERATION

The AAT1267B offers a complete solution for powering TFT LCD panels. The device integrates a boost regulator for the source driver, a buck regulator for the system logic power supply, a positive charge pump regulator for the gate-on driver, a negative charge pump regulator for gate-off, a high voltage switch with gate pulse modulation for flicker compensation, an operational amplifier for supplying the LCD backplane VCOM, a high accuracy high-voltage LDO for gamma reference and various system protection schemes such as soft start, power up sequencing, fault protection, thermal shutdown, and supervisory reset.

Boost Regulator

The boost regulator uses a peak current mode control scheme that provides fast output response during transients, and also simple compensation. With an integrated low R_{DSON} (typical 0.1Ω) NMOS, user controlled soft start, and selectable switching frequency of either 500kHz or 750kHz, this boost regulator is a compact and economical solution but also provides design in flexibility. The boost regulator operates from a minimum input voltage of 8V, and delivers an output voltage by modulating duty cycle D of the internal power NMOS in each switching cycle. The duty cycle is calculated by

$$D = \frac{V_O - V_I}{V_O} \quad \text{or} \quad \frac{V_O}{V_I} = \frac{1}{1-D}, \quad (V_O = V_{AVDD})$$

where V_O (V_{AVDD}) is the output of the boost regulator.

At the heart of the current mode topology are two feedback loops. See the AAT1267B Boost Regulator Functional Block Diagram Figure 1. One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal power switch. The second loop monitors the boost output via a resistive divider to the FB1 pin and compares the FB1 voltage to an internal reference voltage of 1.25V using a transconductance error amp. Regulation is achieved by modulating the internal power switch ON time. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles above 50%. During each rising edge of the internal clock pulse, the power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

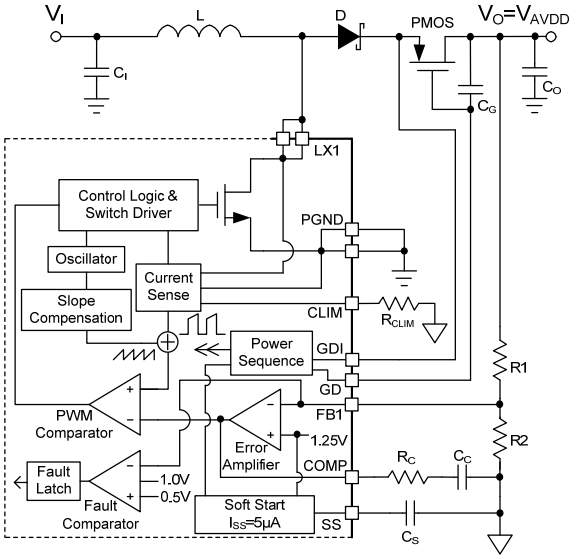


Figure 1. AAT1267B Boost Regulator Functional Block Diagram

Boost Soft Start (t_{SS})

The AAT1267B ramps up the boost regulator's current limit to achieve soft start. Soft start is either performed internally or externally. When the capacitance at the SS is lower than 200pF, soft start is performed internally by stepping up the current limit in 128 steps within 16ms. When the capacitance at SS is larger than 200pF, soft start time is controlled via an external capacitor (C_S) connected from the SS to ground. When V_I is above the UVLO threshold and the EN input is above the enable threshold, an internal 5μA current

source (I_{SS}) will begin to charge the capacitor from 0V to a nominal 1.25V (V_{REF}). The formula is given by

$$C_S = t_{SS} \times \frac{I_{SS}}{V_{REF}}$$

Where I_{SS} = 5µA, V_{REF} = 1.250V.

Boost Current Limit (I_{CLIM})

The boost regulator current limit can be externally adjusted using the CLIM. When CLIM is left floating or R_{CLIM} is larger than 50kΩ, the de fault current limit is 3.6A. A resistor (R_{CLIM}) can also be connected from CLIM to ground to externally set the current limit. Use the following equation to calculate the required current limit.

$$R_{CLIM} = 1{,}000 \times (\frac{I_{CLIM}}{0.085} - 1)$$

GD Function

Power up sequencing and true shutdown is provided for the boost regulator. The GD output drives an external PMOS that is usually placed in the path between the boost Schottky diode and the output filter capacitors. When the enable pin EN is logic low, the GD and GDI are internally connected via a low impedance path, turning off the external PMOS. Note that GDI is connected to the source of the external PMOS. When the EN pin is logic high and the negative charge pump regulator is regulating, the GD output will pull low, turning on the PMOS. Once the GD output toggles low, the boost regulator will be activated and the boost soft start will begin. When the GD function is not used, leave the GD floating and connect the GDI to the boost regulator's output.

Buck Regulator

This device integrates a buck regulator that includes a high side low R_{DSON} (typical 0.1Ω) NMOS switch, pulse width modulation (PWM) controller, built-in soft start, and internal loop compensation. An external bootstrap capacitor of 0.1µF connected from the switch node (LX2) to BST is used to provide the high side gate driver supply. Note that an external Schottky diode rectifier is always required as the internal low side NMOS switch is used for charging the 0.1µF bootstrap capacitor during startup and maintains fixed frequency operation at light load.

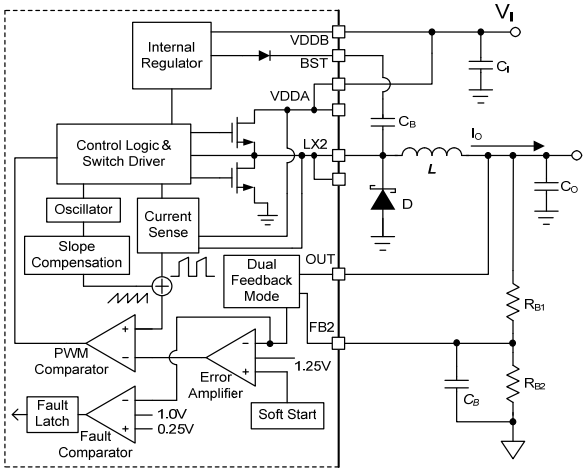


Figure 2. AAT1267B Buck Regulator Functional Block Diagram

The buck regulator uses the peak current mode PWM control scheme for fast transient response and cycle-by-cycle current limiting. The PWM maintains a constant frequency and varies the duty ratio according to the output voltage and load current. This modulation scheme provides high efficiency at medium to heavy load conditions, and reduces the output ripple at light load conditions. It regulates output voltage from V_I down to an output voltage as low as 1.5V. The duty cycle D is calculated by

$$D = \frac{V_O}{V_I} \quad (V_O = V_{BUCK})$$

Where V_O (V_{BUCK}) is the output voltage of the buck regulator. Typical maximum duty cycle is approximately 80%.

In this operating mode, the high side NMOS turns on each cycle for a minimum on-time, and turns off when an internal sawtooth signal exceeds the error amplifier output which monitors the buck output via a voltage resistive divider to the FB2 and compares the FB2 voltage to an internal reference of 1.25V. The sawtooth signal is composed of the sensed inductor current and

an artificial slope compensation ramp to prevent oscillation at duty ratios higher than 50%. After the high side NMOS is turned off, the low-side NMOS is turned on until the next cycle begins.

Buck Soft Start

In order to limit the inrush current during startup, the buck regulator has build in soft start. The soft start period is 3ms and performed internally by stepping up the current limit in 128 steps.

Buck Current Limit

The buck regulator includes cycle by cycle current limiting, with a threshold of typically 3.2A. When the current limit threshold is reached, the high side NMOS switch is turned off, releasing the inductive energy.

Buck Dual Mode Feedback

This buck regulator can be configured for fixed output of 3.3V or adjustable output. For a fixed output of 3.3V, connect the FB2 directly to ground. To set the adjustable output voltage, connect a resistive network from the output (V_O) to ground with the center tap to FB2, as shown in Figure 2. Use the following equation to calculate the required output voltage.

$$R_{B1} = R_{B2} \times (\frac{V_O}{V_{FB2}} - 1)$$

Where V_{FB2} is 1.250V and choose R_{B2} to be between 1kΩ and 50kΩ.

Positive Charge Pump Regulator

The positive regulated charge pump provides a step-up supply for the TFT LCD panel gate-on driver. The achievable output voltage is determined by the number of charge pump stages. For example, for achieving a maximum capable of approximately 3x the input voltage will require a two stage charge pump as shown in Figure 3. However, the actual regulated voltage is set by an external resistive divider from V_{GH} to GND with center tap connected to FBP.

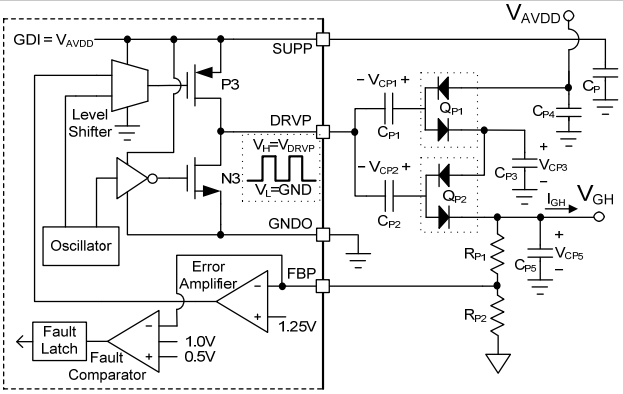


Figure 3. Positive Charge Pump Regulator Functional Block Diagram

The positive charge pump consists of a high side PMOS (P3) and low side NMOS (N3) both controlled by an internal oscillator switching at 500kHz (or 750kHz). Initially, when the oscillator output is logic Low, P3 is turned off while N3 is turned on, pulling the charge pump drive output low (V_{DRVP} = GND), recharging the flying capacitors C_{P1} and C_{P2} by the input supply V_{AVDD} and V_{CP3}. Thus,

$V_{CP1} = V_{AVDD} - V_D$
$V_{CP2} = V_{CP3} - V_D$ where $V_{CP3} = V_{AVDD} - 2V_D + V_{DRVP}$
V_D = the voltage drop across the diode

When the oscillator output is logic High, P3 is turned on while N3 is turned off, pulling the charge pump drive output to a high potential V_{DRVP}, and level shifting the flying capacitors. If the output capacitors are at a lower potential, by more than a diode drop than the level shifted flying capacitors, charge will flow from the flying capacitors to the output capacitors to replenish the output charge. Thus,

$V_{CP3} = V_{AVDD} - 2V_D + V_{DRVP}$
$V_{CP5} = V_{GH} = V_{CP2} - V_D + V_{DRVP}$
$V_{GH} = V_{AVDD} - 4V_D + 2V_{DRVP}$

When V_{DRVP} is approximately equal to V_{AVDD}, the voltage at V_{GH} is approximately 3x the input voltage V_{AVDD}. This is the maximum achievable output voltage for the two stage charge pump.

When the high side PMOS is on while the low side

NMOS is off, the charge pump drive output V_{DRVP} will be pulled high to a voltage magnitude that is dependent on the output power requirement. For example, as the output load increases, the feedback voltage at FBP will initially fall, increasing the error amplifier output drive strength and also the charge pump drive output voltage to a higher level. This increase in voltage of the charge pump drive output high level provides more charge to the flying capacitors and to the output for regulation. Likewise, when the output power demand drops, the charge pump drive output voltage during the high level will decrease.

Charge Pump Flying Capacitors

Use a 0.1µF ~ 0.47µF for the flying capacitors (C_{P1}, C_{P2}) and make sure that the voltage rating (V_{CP}) of these capacitors is adequate per the number of stages. The voltage rating of the capacitor must satisfy

$$V_{CP} > n \times V_{AVDD}$$

where V_{AVDD} is the input supply to the charge pumps, and n is the number of stages per charge pump. Note that the positive charge pump uses 2 stages, i.e. n = 2.

Charge Pump Output Capacitors

The output capacitor (C_{PO}) for the charge pump is selected to satisfy the output ripple requirement. Use ceramics for low ESR to minimize the ripple. The capacitance value can be found by

$$C_{PO} > \frac{I_{GH}}{2 \times f_{OSC} \times \Delta V_{RIPPLE}}$$

where ΔV_{RIPPLE} is the output ripple specification, f_{OSC} is 0.5 x boost operating frequency.

Positive Charge Pump Output Setting

The positive charge pump output voltage (V_{GH}) is set with external resistor ladder from its output to ground with the center tap connected to FBP pin, as shown in Figure 3, Use the following equation,

$$R_{P1} = R_{P2} \times \left(\frac{V_{GH}}{V_{FBP}} - 1\right)$$

Where V_{FBP} is 1.250V, R_{P2} = 10kΩ.

Negative Charge Pump Regulator

The negative regulated charge pump generates a negative supply for the TFT LCD panel gate-off driver. The maximum output voltage capability is determined by the number of charge pump stage, but the actual regulated output voltage is set via a resistive divider to REF, with the center tap connected to FBN. Typical application uses a single stage, as shown in Figure 4. The regulation scheme of the negative charge pump also consist of a high side and low side switch for charging, level shifting the flying capacitor, and drawing charge from the output.

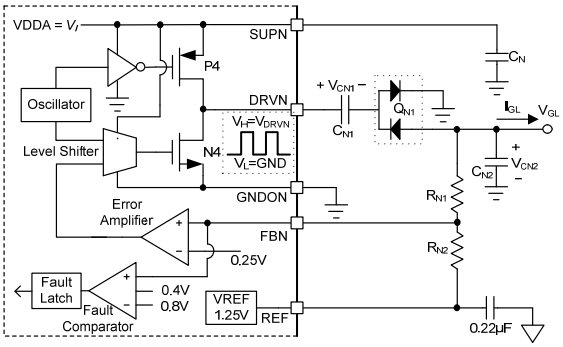


Figure 4. Negative Charge Pump Regulator Functional Block Diagram

When the high side PMOS (P4) is turned on and the low side NMOS (N4) is off, the flying capacitor C_{N1} will charge as the upper diode will turn on and create a path to ground, and $V_{CN1} + V_D = V_{DRVN}$. When the drive output DRVN pulls low to near ground, the flying capacitor C_{N1} is level shifted in the negative direction, and the node connecting between C_{N1} and Q_{N1} becomes ($-V_{CN1}$). Thus, charge will flow from the output C_{N2} to C_{N1}, and the output can be expressed as

$$(-V_{CN1}) = V_{CN2} - V_D \rightarrow V_{CN2} = (-V_{CN1}) + V_D$$
$$V_{CN2} = (-V_{DRVN}) + 2V_D \text{ where } (V_{CN1} = V_{DRVN} - V_D)$$

The voltage magnitude of V_{DRVN} when pulled high will vary, as this voltage is dependent on the output power requirement. The maximum capable output voltage at V_{DRVN} when the P4 is fully turned ON is V_I. Thus, the maximum capable output of this single stage charge pump is

$$V_{GL} = V_{CN2} = (-V_I) + 2V_D$$

Charge Pump Flying Capacitors

Use a 0.1µF ~ 0.47µF for the flying capacitor (C_{N1}) and make sure that the voltage rating (V_{CN}) of these capacitors is adequate per the number of stages. The voltage rating of the capacitor must satisfy

$$V_{CN} > n \times V_{AVDD}$$

where V_{AVDD} is the input supply to the charge pumps, and n is the number of stages per charge pump. Note that the negative charge pump uses 1 stage, i.e. n = 1.

Charge Pump Output Capacitors

The output capacitor (V_{PO}) for the charge pump is selected to satisfy the output ripple requirement. Use ceramics for low ESR to minimize the ripple. The capacitance value can be found by

$$C_{PO} > \frac{I_{GL}}{2 \times f_{OSC} \times \Delta V_{RIPPLE}}$$

where ΔV_{RIPPLE} is the output ripple specification, f_{OSC} is 0.5 x boost operating frequency.

Negative Charge Pump Output Setting

The output voltage (V_{GL}) of the negative charge pump is set with an external resistor ladder from its output to REF pin, with the center tap connected to FBN pin, as shown in Figure 4. Use the following equation to calculate the required output voltage

$$R_{N1} = R_{N2} \times \frac{(V_{GL} - V_{FBN})}{(V_{FBN} - V_{REF})}$$

where V_{FBN} is 0.250V, V_{REF} is 1.250V, and choose R_{N2} to be between 10kΩ and 50kΩ.

High Voltage Switch for Gate Pulse Modulation (GPM)

An internal high voltage switch controller is included for gate pulse modulation which provides gate shaping to improve image quality in TFT LCD applications. The circuitry consist of two high voltage PMOS, one between VGH and VGHM, and another between VGHM and DRN. See Figure 5 for the Gate Pulse Modulation Functional Block Diagram. When the switch controller is enabled, logic level on the GVOFF input will determine which PMOS switch is ON or OFF. If GVOFF is logic High, P5 turns on and P6 turns off, VGHM connects to VGH. If GVOFF is logic Low, P5 turns off and P6 turns on, VGHM connects to DRN, and the V_{GHM} output is discharged via the resistor connected at DRN to ground. V_{GHM} will discharge to 10x the voltage set at THR. Once the V_{GHM} reaches 10 x V_{THR}, P6 will be turned off. Note that the resistor (R_{DRN}) value can be adjusted to different discharge time or high to low transient slope rate.

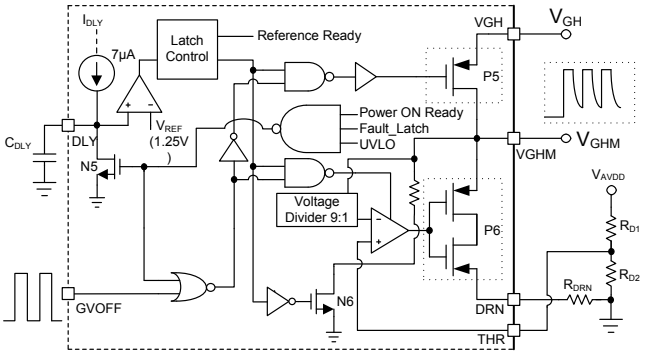


Figure 5. Gate Pulse Modulation Functional Block Diagram

The GPM must be enabled for the GVOFF input to control the PMOS switches. When the device supply voltage has exceeded the UVLO threshold, soft start has completed for V_{BUCK}, V_{GL}, V_{AVDD}, V_{GH} or device is power on ready, and no fault condition is present, an internal 7µA current source will begin to charge the external capacitor connected to the DLY. While this capacitor is charging, the VGHM will be pulled to ground via an internal resistor and NMOS (N6). When the voltage at DLY exceeds V_{REF} (1.25V), the NMOS switch (N6) will be turned off, the GPM will be enabled, and GVOFF will control the PMOS switches as described above.

During operation, if the input supply falls below the UVLO threshold, the GPM will be immediately disabled. Instantly, the high side PMOS P5 will turn on, the low side PMOS P6 will turn off simultaneously, and GVOFF input will have no control over the PMOS switches.

C_{DLY} Time Delay Setting

After device power up and soft start for the four regulators have completed, a 7µA current source will begin charging the external capacitor (C_{DLY}) connected at the DLY to ground. When the voltage at the DLY exceeds V_{REF} (1.25V), the switch control block will be enabled. The capacitor (C_{DLY}) to set the enable delay time (t_D) is chosen using the following formula.

$$C_{DLY} = t_D \times \frac{I_{DLY}}{V_{REF}} \quad \text{where} \quad I_{DLY} = 7\mu A, V_{REF} = 1.250V$$

Discharging Stop Voltage Setting

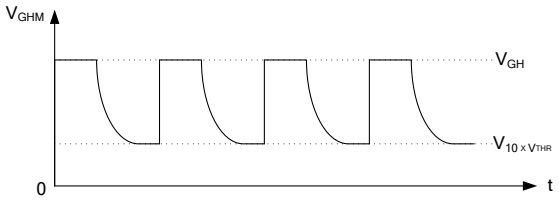


Figure 6.

When the V_{GHM} output reaches 10x the voltage set at THR, P6 will be turned off, and discharging will stop at 10 x V_{THR}, as shown in Figure 6. The 10 x V_{THR} voltage (V_{10VTHR}) can be set via external resistor ladder from V_{AVDD} to GND with the center tap connected to THR, as shown in Figure 5. Use the following equation to calculate the required setting voltage.

$$V_{THR} = V_{AVDD} \times (\frac{R_{D2}}{R_{D1} + R_{D2}}), \quad V_{10VTHR} = 10 \times V_{THR}$$

$$R_{D1} = R_{D2} \times (\frac{10 \times V_{AVDD}}{V_{10VTHR}} - 1)$$

Where R_{D2} = 10kΩ.

Operational Amplifier for VCOM Buffer

The operational amplifier drives the LCD backplane (VCOM) or the gamma-correction divider string. The Op Amp is capable of rail-to-rail input and output, ±200mA output short-circuit current, and a 45V/µs slew rate. In typical application, the inverting input is shorted to the output for a voltage follower (unity gain) configuration.

In the voltage follower configuration, the capacitive load adds a pole to the loop gain that impacts the stability of the system and leads to output peaking, ringing and oscillation. A higher pole frequency results in greater stability. In fact, if the pole frequency is lower than or close to the unity gain frequency, the pole can have a significant negative impact on phase and gain margins. Therefore, the stability decreases when the capacitive load increases.

One method of improving capacitive load drive is to insert a 2Ω to 20Ω resistor (R_{O1}) in series with the output, as shown in Figure 7. This reduces ringing with large capacitive loads while maintaining DC accuracy.

Another method for improving transient response is to add a snubber circuit at the output. A snubber circuit consists of a resistor (R_{O2}) in series with a capacitor (C_{O2}), which improves output settling time and reduces peaking. The advantage of this topology is that it draws no DC current nor does it reduce the gain.

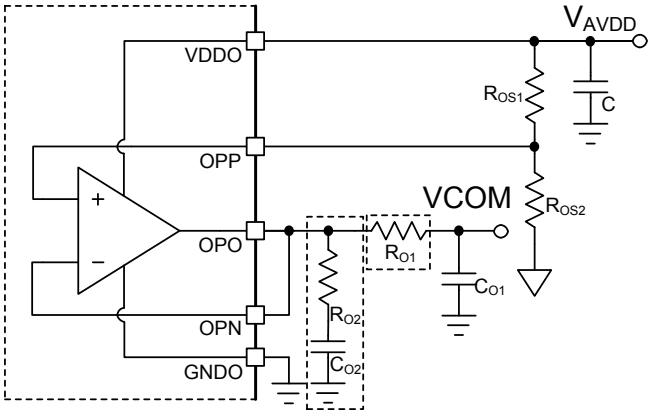


Figure 7. Voltage Follower Operational Amplifier Functional Block Diagram

VCOM Buffer Output Setting

The VCOM Buffer output voltage (VCOM) is set with external resistor ladder from its output to ground with the center tap connected to OPP pin, as shown in Figure 7, Use the following equation,

$$R_{OS1} = R_{OS2} \times (\frac{V_{AVDD}}{V_{COM}} - 1)$$

Where V_{AVDD} is the output voltage of boost regulator, R_{OS2} = 10kΩ.

High Accuracy LDO for Gamma Reference

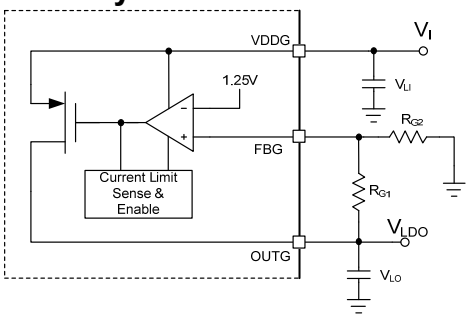


Figure 8. LDO Functional Block Diagram

A high accuracy ±0.5% linear regulator provides a reference to the gamma correction circuitry. This LDO rejects the ripple voltage produced by the source drivers and is capable of providing a minimum 60mA output current, see Figure 8. The output (V_{LDO}) of the LDO is set via a resistive divider from the output to ground, with center tap connected to the FBG pin, with a feedback voltage (V_{FBG}) of 1.250V. Set R_{G2} between 5kΩ to 50kΩ and calculate R_{G1} using the following equation

$$R_{G1} = R_{G2} \times (\frac{V_{LDO}}{V_{FBG}} - 1) \quad \text{where } V_{FBG} \text{ is 1.250V}$$

$\overline{\text{RESET}}$ Function (XAO)

This device has an internal reset circuit to monitor the voltage at VDET. In typical application, the input supply is monitored by connecting a resistive divider from the input (V_I) to ground, with center tap connected to VDET. When the VDET voltage is lower than the threshold voltage of V_{VDET} (1.25V), XAO output will be pulled low. XAO is an open-drain output that needs a pull-up resistor (R_X=10kΩ) to a system supply. The reset circuit is active when the device's internal regulator and reference has exceeded the UVLO threshold.

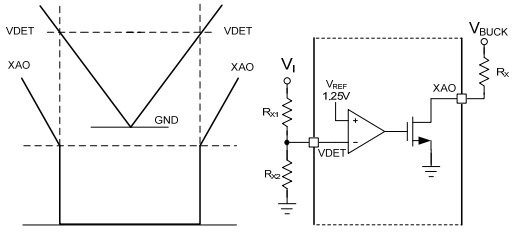


Figure 9. $\overline{\text{RESET}}$ Functional Block Diagram

As shown in Figure 9, use the following equation to calculate the required resisters of R_{X1} and R_{X2}.

$$R_{X1} = R_{X2} \times (\frac{V_I}{V_{VDET}} - 1)$$

where V_{VDET} is 1.250V and R_{X2}=10kΩ.

Reference Voltage (V_{REF})

The reference output voltage is 1.250V. The reference voltage can be used to regulate the negative charge pump and source at least 50μA. In order to have a stable reference voltage, connect a 0.22μF ceramic bypass capacitor between REF and GND.

Operating Frequency Setting

The switching frequency of the Boost and Buck regulators are controlled by the same internal oscillator, but operate 180º out of phase from each other for reducing the input RMS current. The operating frequency can be set by FSEL. If FSEL is connected to V_I or is floating, the operating frequency is 750kHz. If FSEL is connected to GND, the operating frequency is 500kHz.

Power On/Off Sequence

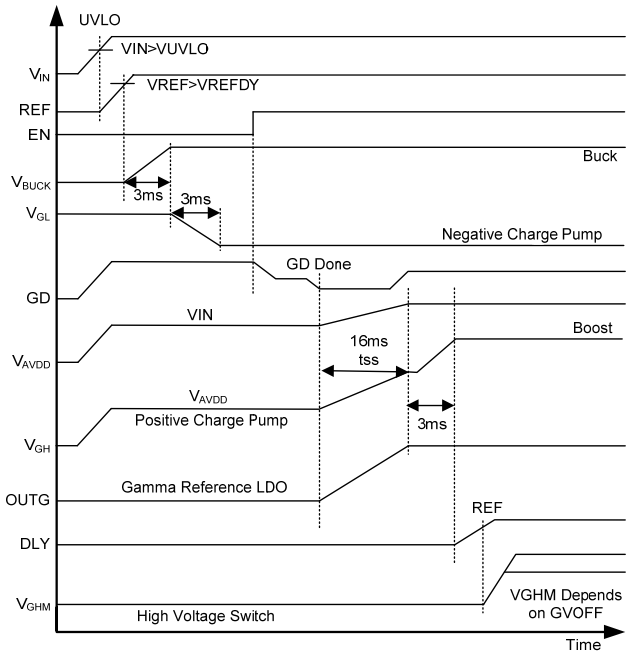


Figure 10. AAT1267B Power up Sequence

The AAT1267B Power up Sequence is as shown in Figure 10. When V_{IN} exceeds the UVLO threshold, and the internal reference (V_{REF}) is ready, the buck regulator (V_{BUCK}) first powers up. Once the buck regulator has completed its soft start and is in regulation, the negative charge pump (V_{GL}) begins to power up. When the EN input is logic high, the GD output starts to turn on the external PMOS. Once GD has completely turned on the external PMOS, the boost regulator (V_{AVDD}) and the gamma reference LDO (OUTG) will be simultaneously activated. The positive charge pump (V_{GH}) will only begin to turn on when the boost has completed its soft start. Also note that the high voltage switch (V_{GHM}) controller's enable delay time is dictated by the DLY capacitor charging up after the positive charge pump has completed.

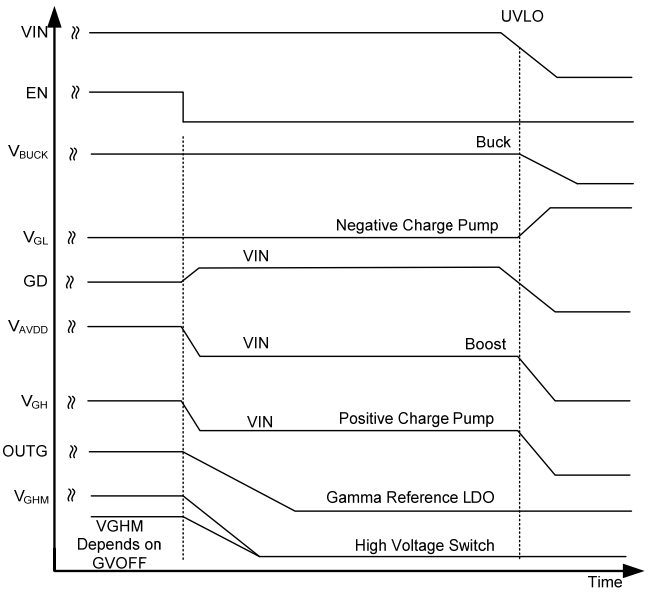


Figure 11. AAT1267B Power off Sequence

When the EN input is logic Low, the GD output will turn off the external PMOS, the boost regulator, positive charge pump, gamma reference LDO and the high voltage switch controller will be shutdown. Once V_{IN} drops below the UVLO threshold, the buck regulator and the negative charge pump will be inactivated simultaneously, see the Figure 11 for AAT1267B power off Sequence.

Fault Protection

The device fault protection feature is described in Table 1. If short circuit protection (SCP) is triggered by any of the four regulators (boost, buck, V_{GH}, V_{GL}), no fault timer is applied, the part latches off immediately. If any one of the four regulators' feedback voltage is lower than its Fault Protection Voltage threshold (UVP), an internal fault timer of 50ms is activated. Once activated, if the fault condition surpasses the 50ms, the device will shutdown all regulators but will keep the internal reference at 1.25V. Note that fault protection is only active after all soft start events have completed. When the device is shutdown due to a fault condition, the power supply to the device must be recycled in order to restart the device.

Thermal Shutdown

The AAT1267B device enters into fault protection shutdown when the junction temperature reaches approximately 160°C. To restart the device when the junction temperature has fallen below the thermal shutdown threshold, recycle the device supply power below the UVLO falling threshold.

Channel	Fault Condition Type	Description of Fault Condition	Channels Disabled Due to Fault
Boost (V_{AVDD})	OCP	LX1 stop switching until current lower than OCP level	
	OVP	LX1 stop switching until voltage lower than OVP level	
	SCP	FB1 falls below 0.5V, channel shuts down immediately	V_{AVDD}, V_{GH}, V_{GL}
	UVP	FB1 falls below 1V for more than 50ms	
Buck (V_{BUCK})	OCP	LX2 stop switching until current lower than OCP level	
	SCP	FB2 falls below 0.25V, channel shuts down immediately	V_{BUCK}, V_{AVDD}, V_{GH}, V_{GL}
	UVP	FB2 falls below 1V for more than 50ms	
V_{GH}	SCP	FBP lower than 0.5V, channel shuts down immediately	V_{AVDD}, V_{GH}, V_{GL}
	UVP	FBP falls below 1V for more than 50ms	
V_{GL}	SCP	FBN rises above 0.8V, channel shuts down immediately	V_{AVDD}, V_{GH}, V_{GL}
	UVP	FBN rises above 0.4V for more than 50ms	

APPLICATION NOTE

Boost Regulator

The AAT1267B integrates a current-mode, PWM Boost and NMOS switch. Figure A1 shows the AAT1267B Boost Regulator Functional Block Diagram.

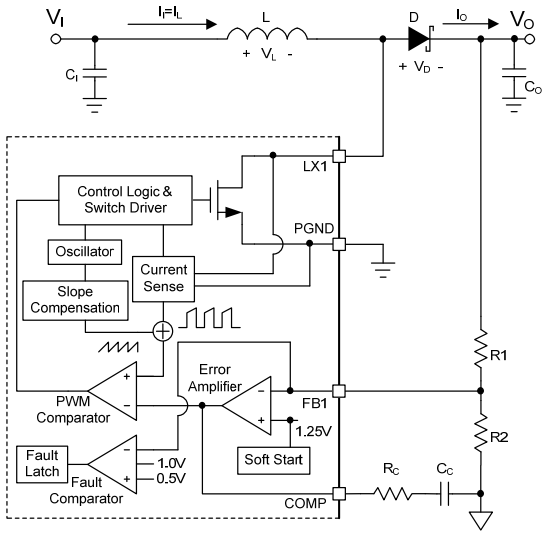


Figure A1. Boost Regulator Functional Block Diagram

The boost regulator steps the input voltage up to higher output voltage. The basic configuration of a boost regulator can be seen in Figure A2.

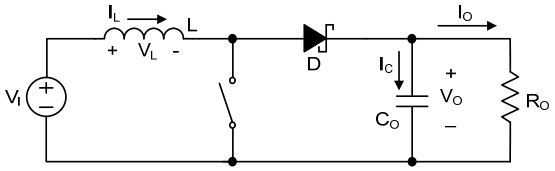
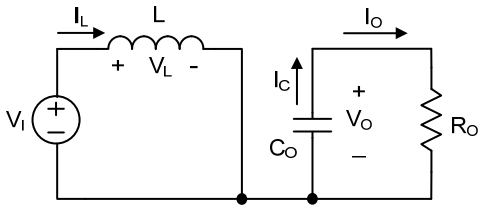


Figure A2. Basic Boost Regulator Topology

The basic boost regulator operates in two time periods. The first time duration (DT_S) occurs when the switch is on, and the diode is reversed biased. This results in a positive voltage $V_L=V_I$ across the inductor. This voltage causes a linear increase in the inductor current I_L. During this "ON" period, energy is stored in the inductor and the load current is supplied by C_O.



Switch Off For The Time Duration DT_S

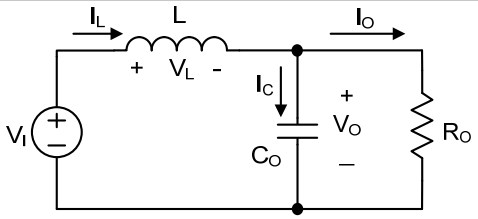


Figure A3. Switch Off For The Time Duration (1-D)T_S

The next time duration is the "OFF" period of the power switch. When the switch is turned off, the diode is forward biased, and the energy stored in the inductor is transferred to the load and output capacitor. The voltage across the inductor reverses its polarity and is clamped by the diode, because of the inductive energy storage, I_L continues to flow. The current now flows through the diode, and $V_L = -(V_O - V_I)$ for a time duration $(1\text{-}D)T_S$ until the switch is turned on again.

Equating the integral of the inductor voltage over one time period to zero yields

$$\int_0^{T_S} V_L(t)dt = \int_0^{DT_S} V_L(t)dt + \int_{DT_S}^{T_S} V_L(t)dt,$$

$$\left(D = \frac{t_{ON}}{T_S} \text{ where } T_S \text{ is the period of switching}\right)$$

$$V_I \times DT_S - (V_O - V_I) \times (1-D)T_S = 0$$

$$V_I = (1-D)V_O, \quad \frac{V_O}{V_I} = \frac{1}{1-D}$$

Component Selection for Boost Regulator

Inductor Selection (L)

The value of the inductor is calculated based on the input V_I and output voltage V_O, switching frequency f_{OSC}, and the nominal output load current I_O. However, when selecting the optimal inductance, both the regulator's performance and the inductor size or cost must be considered. According to the operating relationship between inductor voltage and inductor current shown in Figure A4, the Inductor ripple current (ΔI) can be calculated by the following equation.

$$iL(t) = iL(0) + \frac{1}{L}\int V_L(t)dt, \quad \left(T_S = \frac{1}{f_{OSC}}, \quad \frac{V_O}{V_I} = \frac{1}{1-D}\right)$$

$$\Delta I = \frac{1}{L} V_I \times DT_S = -\frac{1}{L}(V_O - V_I) \times (1-D)T_S$$

$$\Delta I = \frac{1}{L} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I)$$

And obtain Inductance L

$$L = \frac{1}{\Delta I} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I),$$

$$\left(\eta = \frac{V_O \times I_O}{V_I \times I_I}, \quad L_{IR} = \frac{\Delta I}{I_I} = \frac{\eta \times V_I}{V_O \times I_O} \times \Delta I\right)$$

$$L = \frac{\eta}{L_{IR}} \times \frac{1}{f_{OSC}} \times \left(\frac{V_I^2 \times (V_O - V_I)}{V_O^2 \times I_O}\right)$$

Where L_{IR} is the ratio of the ripple current (ΔI) to input current (I_I) at the full load current, and η is efficiency.

Although using a small inductance can decrease component size or cost and increase the regulator's response time, inductor ripple current increases which results in high output ripple and in lower efficiency due to increase conduction losses. Using a large inductance can lower ripple current to mitigate conduction losses and minimize output ripple, but too large of an inductance leads to slow response time and lower efficiency if the losses from the higher DCR outweigh the losses eliminated from lower ripple current. The inductor ripple current is usually adjusted by the system designer based on application for the desired cost and performance.

After selecting the inductance value, the inductor's saturation current rating should be chosen to exceed the inductor ripple current for the lowest input voltage V_{I_MIN} in the application.

$$I_{L\_AVE(MAX)} = \frac{V_O \times I_O}{V_{I\_MIN} \times \eta} \quad \left(\text{where } \eta = \frac{V_O \times I_O}{V_I \times I_I}\right)$$

And Inductor peak current I_{L_PEAK}

$$I_{L\_PEAK} = I_{L\_AVE(MAX)} + \frac{1}{2}\Delta I$$

$$I_{L\_PEAK} = \frac{V_O \times I_O}{V_{I\_MIN} \times \eta} + \frac{1}{2L} \times \frac{1}{f_{OSC}} \times \frac{V_I}{V_O}(V_O - V_I)$$

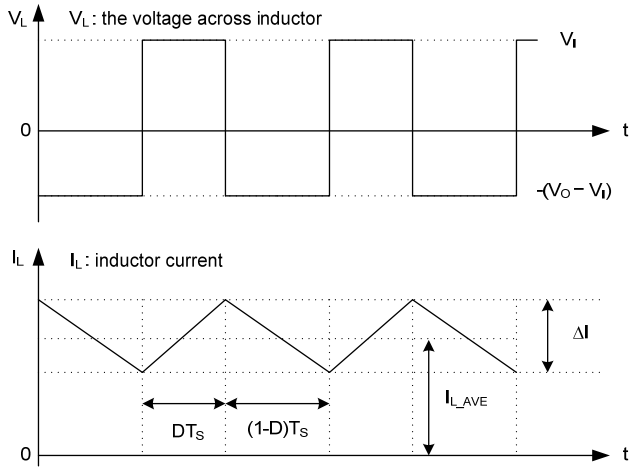


Figure A4. Inductor Voltage vs. Inductor Current (CCM)

For boost regulator, L_{IR} is usually chosen to be 0.3 to 0.5. However, if the inductor used in the TFT LCD application has significant wire resistance, higher L_{IR} (above 0.5) can be used to lower the inductance value and therefore lower the total DCR.

Output Capacitor Selection (C_O)

For switching regulators, output capacitance is chosen based on the desired output ripple and/or output voltage deviation based on a given load change.

The output voltage ripple consists of both the inductor ripple current flowing through the capacitor ESR (equivalent series resistance), and the transfer of charge to and from the output capacitor. Since in TFT LCD display applications, ceramic capacitors are used at the output, the ripple due to the IR effect can be neglected since ceramics capacitors have extremely low ESR. Thus the ripple due to the charge and discharge of the output capacitor will be dominant. Based on a desired ripple, the minimum output capacitance can be calculated by. (Please refer to the Figure A5)

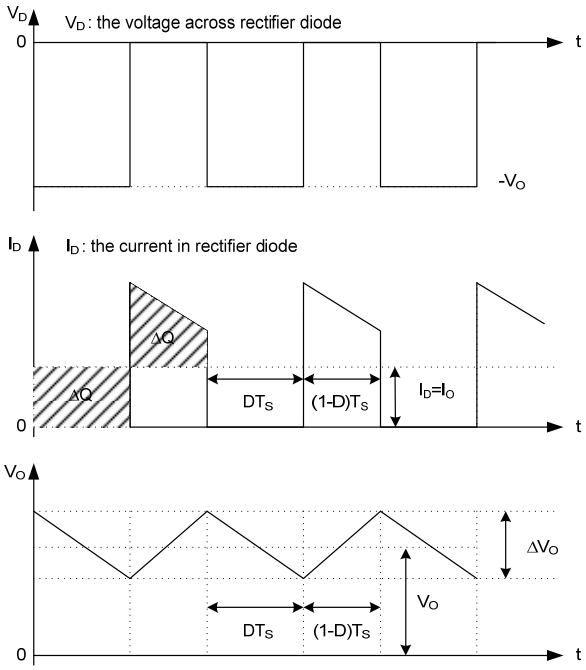


Figure A5.

$$\Delta V_O = \frac{\Delta_Q}{C_O} = \frac{I_O \times DT_S}{C_O} \left(Q = C_V, T_S = \frac{1}{f_{OSC}}, \frac{V_O}{V_I} = \frac{1}{1-D} \right)$$

$$\Delta V_O = \frac{I_O}{C_O} \times \frac{1}{f_{OSC}} \times \frac{(V_O - V_I)}{V_O}$$

$$C_O = \frac{I_O}{\Delta V_O} \times \frac{1}{f_{OSC}} \times \frac{(V_O - V_I)}{V_O}$$

where ΔV_O is the output ripple voltage specification.

Note that ceramic capacitors are often used for their size advantage and environmentally-friendly nature. To achieve the required ripple or output capacitance value, multiple ceramic capacitors are often connected in parallel.

Input Capacitors Selection (C_I)

Input capacitors are usually a combination of bulk capacitor and high frequency ceramic. The bulk capacitor serves as the power source during the soft start process, supplies switching current, minimizes input ripple, and keeps the DC input voltage stable. The bulk capacitor is usually chosen to support the input RMS current, and can also be ceramic type. Often, extra bulk capacitance is added during bench

evaluation to alleviate the parasitic inductance introduced from the power supply cable.

The high frequency ceramic capacitor filters the high frequency noise to the device. Usually, a 0.1µF to 1µF ceramic capacitor is used. A RC low-pass filter is often added to decrease interference from noise.

Diode Selection (D)

The diode voltage rating must be greater than the output voltage V_O and the current rating must exceed the inductor peak current I_{L_PEAK}. Using a diode with low forward voltage drop and fast recovery time to minimize the conduction loss and switching loss, and then help increase efficiency, such as a Schottky rectifier is recommended.

Output Voltage Selection (V_O)

The output voltage is set using a resistive voltage divider from the output to FB1, referenced to analog ground as shown in Figure A1. Use the following equation to set the boost voltage, or V_O,

$$R_1 = R_2 \times (\frac{V_O}{V_{FB1}} - 1)$$

where V_{FB1} is 1.250V and R_2=10kΩ.

Crossover Frequency Selection

The crossover frequency, or the regulator bandwidth, is usually selected to satisfy the output step load requirement. However, due to the inherent nature of the CCM boost, a right-half-plane-zero (RHPZ) will limit the selection of the crossover frequency (f_C) due to its phase lag. A good design rule is to select the crossover frequency to be about 20% of the RHPZ frequency. The RHPZ frequency is given by

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad \text{where} \quad R_O = \frac{V_O}{I_O}$$

$$f_C = 0.2 \times f_{RHPZ}$$

Compensation Selection (R_C & C_C)

To stabilize the boost regulator's loop, a RC series network is added from the COMP output pin to analog ground. See Figure A1. R_C is chosen to set the amplifier gain for a targeted crossover frequency. Setting the total loop gain to unity gain at the desire crossover frequency, we can calculate R_C by approximately

$$R_C = 0.3 \times \frac{V_O}{V_{FB1}} \times \frac{V_O}{V_I} \times \frac{\pi \times f_C \times C_O}{g_m \times g_{CS}}$$

Where g_m=105µS is the feedback error amplifier transconductance, g_{CS}=4S is the current sense transconductance, the crossover frequency of the regulator f_C=20%×f_{RHPZ}, and V_{FB1} is the feedback reference voltage of 1.24V. In typical application, RC value ranges from 10kΩ to 100kΩ.

Once R_C is selected, C_C is adjusted to place a zero for neutralizing the output pole caused by the output capacitance C_O and load R_O. Use the following equation to calculate C_C,

$$C_C = \frac{C_O \times R_O}{50 \times R_C}$$

In typical application, C_C value ranges from 680pF to 2.2nF.

Buck Regulator

The AAT1267B integrated a current-mode, PWM Buck Regulator. Figure B1 shows the AAT1267B Buck Regulator Functional Block Diagram.

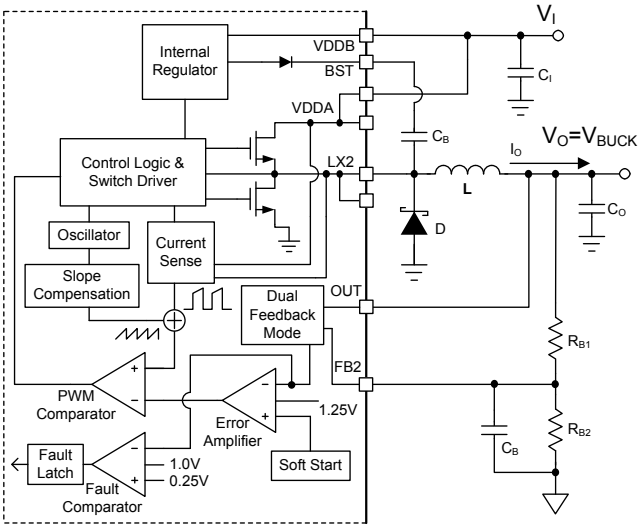


Figure B1. Buck Regulator Functional Block Diagram

The Buck Regulator is the most elementary forward–mode regulator. Its basic schematic can be seen in Figure B2.

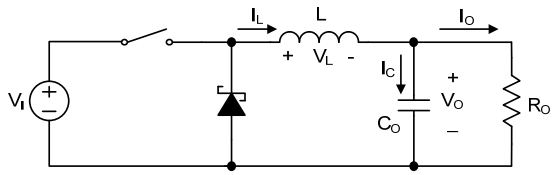
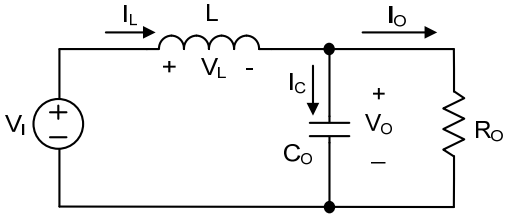


Figure B2. Basic Buck Regulator Topology

The operation of this regulator topology has two distinct time periods. The first one occurs when the switch is on for the time duration DT_S, the switch conducts the inductor current and the diode becomes reverse biased. This results in a positive voltage $V_L = V_I - V_O$ across the inductor. This voltage causes a linear increase in the inductor current I_L. During this "ON" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to supply the requirements of the load during the "OFF" period.



Switch On for the Time Duration DT_S

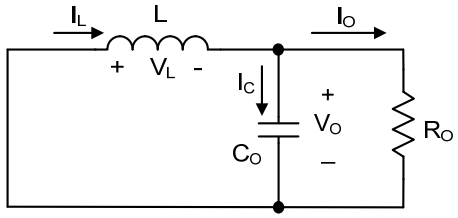


Figure B3. Switch Off For the Time Duration (1-D) T_S

The next period is the "OFF" period of the power switch. When the switch is turned off, the voltage across the inductor reverses its polarity and is clamped by the diode, because of the inductive energy storage, I_L continues to flow. The current now flows through the diode, and $V_L = -V_O$ for a time duration $(1–D)T_S$ until the switch is turned on again. Equating the integral of the inductor voltage over one time period to zero yields

$$\int_0^{T_S} V_L(t)dt = \int_0^{DT_S} V_L(t)dt + \int_{DT_S}^{T_S} V_L(t)dt,$$

$$(D = \frac{t_{ON}}{T_S} \text{ where } T_S \text{ is the period of switching})$$

$$(V_I - V_O) \times DT_S + (-V_O) \times (1-D)T_S = 0$$

$$V_O = DV_I, \quad \frac{V_O}{V_I} = D$$

Assuming a lossless circuit $P_I = P_O$, Therefore

$$P = V_I \times I_I = V_O \times I_O, \text{ and } \frac{I_O}{I_I} = \frac{V}{V_O} = \frac{1}{D}$$

For a buck regulator, it is obvious that

$I_L = I_O$

According to the buck operating relationship between inductor and output capacitor, shown in Figure B4, The peak-to-peak inductor current ripple ΔI_L can be calculated by following equation.

$$i_L(t) = i_L(0) + \frac{1}{L}\int V_L(t)dt, \qquad (T_S = \frac{1}{f_{OSC}}, \quad \frac{V_O}{V_I} = D)$$

$$\Delta I_L = \frac{1}{L}\left[\text{Shaded area under waveform } V_L \text{ (Area A)}\right]$$

$$\Delta I_L = \frac{1}{L}(V_I - V_O) \times DT_S = \frac{1}{L}(-V_O) \times (1-D)T_S$$

$$\Delta I_L = \frac{1}{L} \times \frac{1}{f_{OSC}} \times \frac{V_O}{V_I}(V_I - V_O)$$

From ΔI_L, we can obtain I_{L_MIN} and I_{L_MAX}

$$I_{L\_MIN} = I_L - \frac{\Delta I_L}{2}$$

$$I_{L\_MAX} = I_L + \frac{\Delta I_L}{2}$$

The peak-to-peak output voltage ripple, ΔV_O

$$\Delta V_O = \Delta V_C = \frac{1}{C}\int IC(t)dt, \qquad (Q = C \times V)$$

$$\Delta V_O = \frac{1}{L}\left[\text{Shaded area under waveform } I_L \text{ (Area B)}\right]$$

$$\Delta V_O = \frac{1}{C} \times \frac{1}{2} \times \frac{T_S}{2} \times \frac{\Delta I_L}{2}$$

$$\Delta V_O = \frac{1}{8} \times \frac{1}{f_{OSC}} \times \frac{\Delta I_L}{C}$$

Component Selection for Buck Regulator

Inductor Selection (L)

The inductance (L), saturation current rating and DC resistance (DCR) of the inductor are important parameters to consider when selecting the inductor, since these parameters affect the regulator's performance and efficiency. Base on the input V_I and output voltage V_O, switching frequency f_{OSC}, and the output load current I_O, the inductance (L) can be calculated by the following equation.

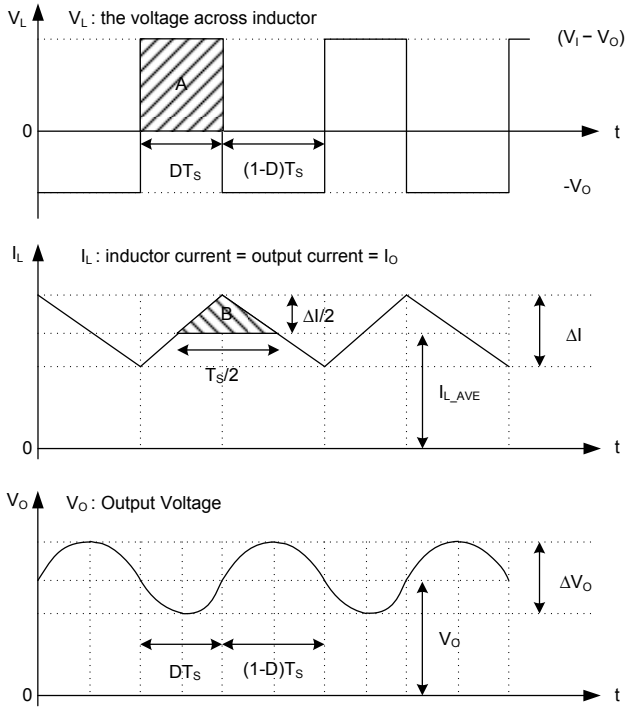


Figure B4. The operating waveform of a Buck Regulator

$$\Delta I_L = \frac{1}{L} \times \frac{1}{f_{OSC}} \times \frac{V_O}{V_I}(V_I - V_O)$$

$$L = \frac{1}{L_{IR} \times I_O} \times \frac{1}{f_{OSC}} \times \frac{V_O}{V_I}(V_I - V_O), \quad \left(L_{IR} = \frac{\Delta I}{I_O}\right)$$

Where L_{IR} is the ratio of peak to peak inductor current ripple (ΔI) to the load current I_O, and is usually set at 20%~40% of I_O. Although using a lower inductance minimizes physical size and cost, a lower inductance increases inductor current ripple and reduces the efficiency due to higher peak currents. On the other hand, a higher inductance reduces the ripple current to mitigate conduction losses and minimize output voltage ripple, but too large of an inductance leads to slow response time and lower efficiency if the losses from the higher DCR outweigh the losses eliminated from a lower ripple current.

Peak current through the inductor determines the inductor's required saturation current rating, the maximum inductor current I_{LMAX} as shown below.

$$I_{LMAX} = I_O + \frac{\Delta I_L}{2}$$

During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For these reasons, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

The DC resistance is the wire resistance of an inductor, and will result in power dissipation due to the current flowing through the inductor. Hence, the inductor DCR should be kept low for good efficiency.

Input Capacitor Selection (C_I)

The input current of the buck regulator is discontinuous, and depending on the load input peak currents can be large, causing large input voltage ripple and noise. Hence the input capacitor must be able to support the maximum input operatin voltage and the maximum RMS input current. Since the input capacitor has to absorb switching current, it requires an adequate ripple current rating. The RMS input current (I_{I_RMS}) can be calculated as follows.

$$I_{I\_RMS} = \frac{I_O}{V_I} \times \sqrt{V_O(V_I - V_O)}$$

In the worst case, with a duty cycle of 50%,

$$D = \frac{1}{2} = \frac{V_O}{V_I}, \quad I_{I\_RMS} = \frac{I_O}{V_I} \times V_O = \frac{I_O}{2}$$

For best performance, use a low ESR input capacitor to prevent large voltage transients from appearing at the input, and to minimize power dissipation. A ceramic type capacitor is recommended because of their high RMS current rating and low ESR for a given physical dimension.

Output Capacitor Selection (C_O)

The output capacitor (C_O) functions to store energy, to maintain the output voltage, and to stabilize the regulation control system. The output capacitor is chosen to meet the output ripple specification and to provide storage for load transients. The ESR of the output capacitor and the peak–to–peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value (ΔV_O). The output ripple voltage is approximated by

$$\Delta V_O = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_O} \right)$$

For low output ripple voltage, low ESR output capacitors are recommended. When a low ESR ceramic capacitor is used, the output voltage ripple due to the ESR is small and can be ignored. In this case the output ripple is mainly attributed to the capacitor charging and discharging. Note that choosing a capacitor with very low ESR may cause the regulator system to be unstable.

The desired output voltage change during a load transient also determines the output capacitance requirement. For a given voltage change ΔV_O, and a given load change ΔI_O, the output capacitance (C_O) can be calculated by

$$C_O = \frac{L \times \left(I_O + \frac{1}{2} \Delta I_O \right)^2}{\left(\Delta V_O + V_O \right)^2 - V_O^2}$$

Where ΔI_O is the change in output current, and ΔV_O is the allowable change in the output voltage.

Rectifier Diode Selection (D)

Since the rectifier diode is a very significant source of power loss in switching power supplies, Schottky diodes are recommended for most application because of their fast recovery time and low voltage drop. Choose a rectifier with a peak voltage greater than the maximum input voltage, and the peak current rating should exceed the maximum inductor current.

Bootstrap Capacitor Selection (C_B)

A 0.1μF ceramic capacitor must be connected between the BST to LX2 pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10V or higher voltage rating.

Output Voltage Selection (V_O)

The buck output voltage is set by an external resistive voltage divider (R_{B1} and R_{B2}), and an internal reference voltage. The external resistive voltage divider feeds the dc output voltage, and an error amplifier compares it with an internal reference voltage V_{FB2} (See Figure B1). The buck output voltage can be calculated from the following equation.

$$R_{B1} = R_{B2} \times \left(\frac{V_O}{V_{FB2}} - 1 \right)$$

where V_{FB2} is 1.250V typical. If R_{B2} is chosen as 1.2 kΩ, R_{B1} is calculated to be 19.8kΩ for an output voltage of 3.3 V.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1267B.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VDDB and REF pins. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VDDB and REF bypass capacitor should referenced to analog ground (GND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost and buck regulator contain the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node LX1 and LX2. The input bulk capacitance should also be placed close to these power path components to shorten the power ground length between the input and output.

Feedback and Compensation Components

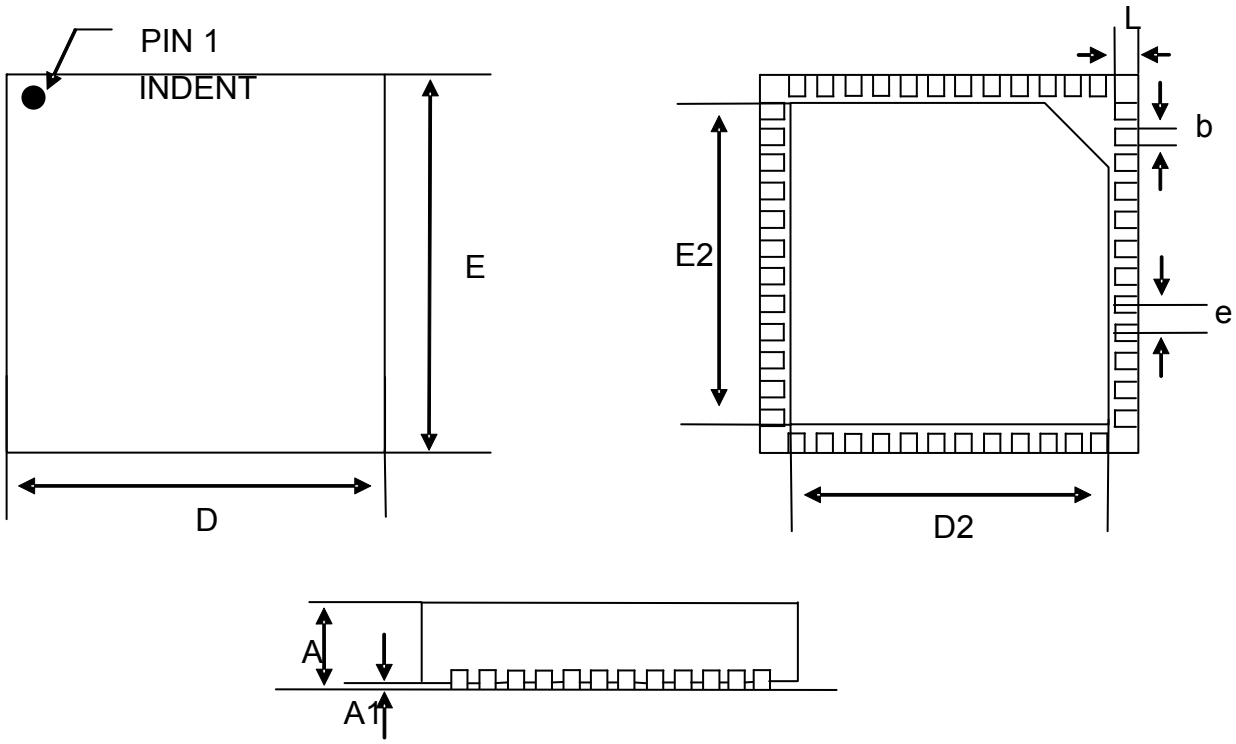
Any components for feedback, such as the resistive divider networks for setting the output voltage, should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise pickup. Likewise, compensation components should be place as close as possible to the pin or device.

Ground Plane

Use a power ground plane for the boost and buck output capacitor ground, for the boost and buck input bulk capacitor ground, charge pump output capacitor grounds, and PGND, GNDO, GNDON pins. All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create an analog ground plane for VDDB and REF bypass capacitor grounds, compensation component ground, feedback resistive network grounds, DLY capacitor ground, VDET ground reference, and also the GND pins. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (GND) and power ground (PGND, GNDO, GNDON) should be connected only at one signal point, near the expose pad by shorting the PGND, GNDO, GNDON pins to the expose pad.

PACKAGE DIMENSION

WQFN48-7X7



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.18	0.25	0.3
D	6.9	7	7.1
D2	5.6	5.7	5.8
E	6.9	7	7.1
E2	5.6	5.7	5.8
e	-----	0.5	-----
L	0.3	0.4	0.5