MULTI-CHANNEL POWER SUPPLY FOR TFT LCD PANELS

FULLY I²C INTERFACE CONTROL – TWO BOOST, CHARGE PUMP, BUCK/LDO GPM, PVCOM, TWO OPERATIONAL AMPLIFIER, RESET

FEATURES

- **2.5V to 5.5V Input Supply Voltage Range**
- **Fully I²C Interface Control**
- **Current Mode Boost Regulator for V_{AVDD}**
  - **3.6V to 12.7V Output Voltage Range**
- **Current Mode Boost Regulator for V_{GH}**
  - **10V to 37V Output Voltage Range**
  - **Temperature Compensation (T/C)**
- **Alternative Buck Regulator or Low Dropout Linear Regulator for V_{25}**
  - **1.5V to 3.0V Output Voltage Range**
- **Negative Charge Pump Linear Regulator for V_{GL}**
  - **-4.5V to -8.0V Output Voltage Range**
- **Unit-Gain Buffer for V_{COM}**
  - **7 Bits, 128-Step Adjustable Sink Current Output**
  - **±200mA Short-Circuit Current**
  - **12V/μs Slew Rate**
  - **Temperature Compensation (T/C)**
- **Two Operational Amplifier**
  - **±120mA Short-Circuit Current**
  - **12V/μs Slew Rate**
- **Gate Pulse Modulation (GPM)**
- **RESET Output (XAO)**
  - **Open Drain Output**
- **Protection**
  - **Over Voltage Protection (OVP)**
  - **Under Voltage Protection (UVP)**
  - **Short Circuit Protection (SCP)**
  - **Over Temperature Protection (OTP)**
- **WQFN 28-3.5mmX5.5mmX0.75mm Package**

GENERAL DESCRIPTION

The AAT1277 is a highly integrated power management IC for TFT LCD panels. The device consists of two current mode boost regulators, a current mode buck regulator or a low dropout linear regulator alternatively, a negative charge pump linear regulator, a gate pulse modulation, a reset function, a unit-gain VCOM buffer and two operational amplifiers. The AAT1277 also includes I²C interface for setting various parameters such as each regulator's output voltage, switching frequency, soft start time, delay times, etc.

The AAT1277 includes a current mode synchronous boost regulator that provides a fast transient response supply voltage for the source driver. The source driver boost is capable of generating up to 12.7V. A second current mode non-synchronous boost supplies the gate-on voltage, and is capable of an output voltage of up to 37V. The VGH boost includes a temperature compensation function. For improving TFT LCD image quality, a gate pulse modulation (GPM) circuit shapes the gate-on signal. The slope of the gate-on voltage can be set by external resistor.

The logic power voltage (V25) could be supplied either by the buck regulator or by LDO alternatively and programmed via I²C from 1.5V to 3V. The synchronous current mode buck regulator operates at a fixed switching frequency of 1.2MHz, and provides fast load transient response to pulsed loads while producing efficiencies over 90%. The low dropout linear regulator (LDO) output voltage guarantees a minimum 350mA output current limit.

The AAT1277 negative charge pump linear regulator generates VGL supply voltage for the gate-off voltage.

The programmable operational amplifier drives the LCD backplane (VCOM). This unity-gain buffer is capable of

rail-to-rail input and output, ±200mA output short-circuit current, and a 12V/µs slew rate. Output voltage can be programmed by I^2C interface using 7-bits or 128 steps, eliminating mechanical potentiometers to reduce labor cost.

Two operational amplifiers are included for the Panel repair-line. Those are not controlled by I^2C interface and their outputs are set using an external signal.

The reset functions (RESET) is used to monitor the V25 voltage. The reset signal is issued via an open drain NMOS when the supply is below a programmable thresholds voltage.

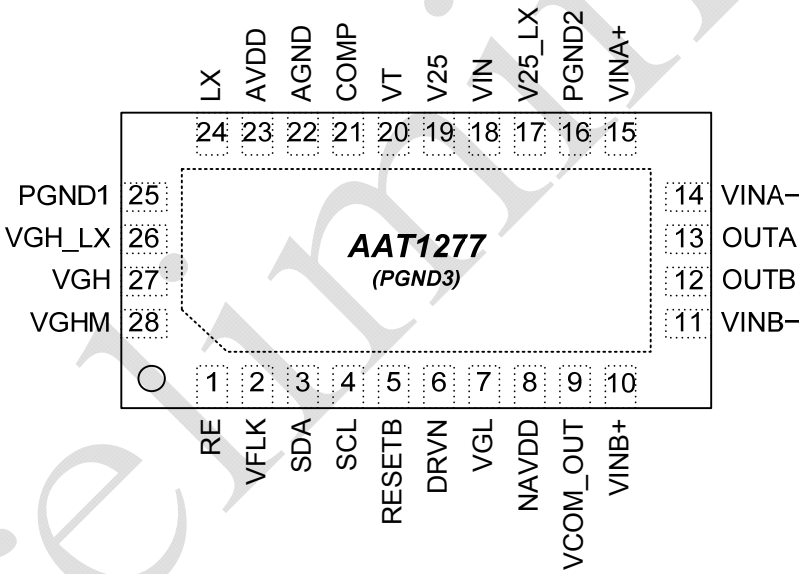
The AAT1277 device includes various protection features such as input under-voltage lockout (UVLO) and over temperature shutdown (OTP). Regulator outputs include under voltage protection (UVP), overload voltage protection (OVP), and short circuit protection (SCP).

The AAT1277 is available in a small WQFN 28 pin 3.5mmX5.5mmX0.75mm with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40 to +85°C temperature range.

APPLICATIONS

- **Tablet Panel**
- **Notebook Panel**

PIN CONFIGURATION

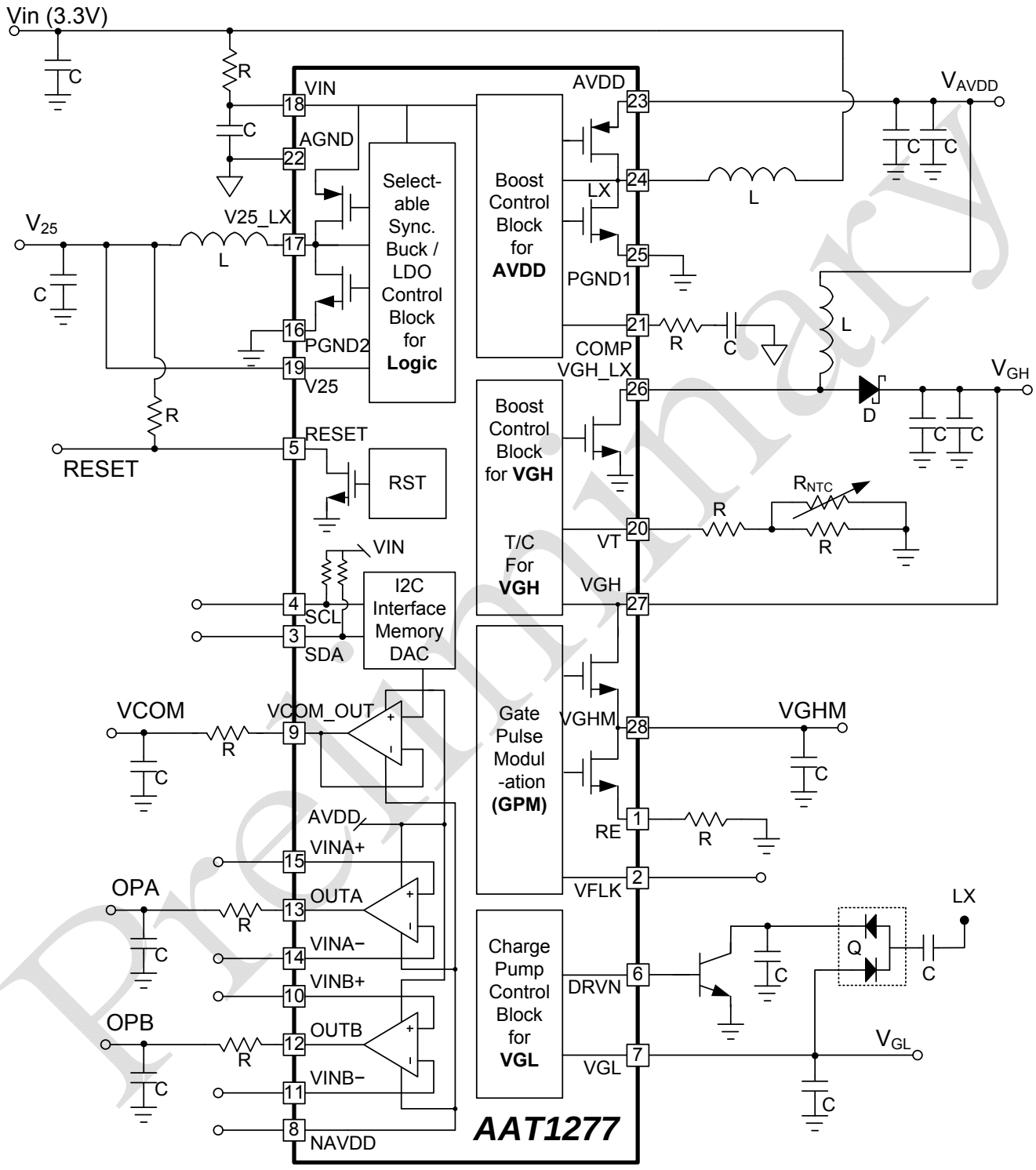


ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1277	AAT1277 -Q45-T	Q45: WQFN28-3.5X5.5	T: Tape and Reel	–40°C to +85°C	1277 XXXXXX XXXX	Device Type Lot no. (6~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VIN to AGND	V_{IN}	–0.3 to +6.5	V
PGND1, PGND2 to AGND	-	–0.3 to +0.3	V
LX to PGND1	V_{H1}	–0.3 to +16.0	V
V25_LX to PGND2	V_{H2}	–0.3 to +6.5	V
VGH_LX to PGND1	V_{H3}	–0.3 to +45.0	V
DRVN to PGND1	V_{H4}	–12.0 to +0.3	V
Input Voltage 1 (SCL, SDA, V25, VFLK)	V_{I1}	–0.3 to V_{IN} +0.3	V
Input Voltage 2 (AVDD)	V_{I2}	–0.3 to V_{H1} +0.3	V
Input Voltage 3 (NAVDD)	V_{I3}	V_{H4} –0.3 to +0.3	V
Input Voltage 3 (VGH)	V_{I4}	–0.3 to V_{H3} +0.3	V
Input Voltage 4 (VGL)	V_{I4}	V_{H4} –0.3 to +0.3	V
Output Voltage 1 (COMP, VT, RESETB)	V_{O1}	–0.3 to V_{IN} +0.3	V
Output Voltage 2 (VCOM_OUT, OUTA, OUTB, VINA+, VINB+, VINA–, VINB–)	V_{O2}	V_{H4} –0.3 to V_{H1} +0.3	V
Output Voltage 3 (VGHM, RE)	V_{O3}	–0.3 to V_{H3}+0.3	V
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Resistance	θ_{JA}	31.88	°C /W
Power Dissipation, @ T_A = +25°C , T_J = +125°C	P_d	3.137	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note:
1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
2. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN Input Voltage Range	V_{IN}		2.5	-	5.5	V
Under Voltage Lockout Threshold	V_{UVLO}	Rising	2.30	2.35	2.40	V
		Falling	2.1	2.2	2.3	V
		Hysteresis	100	150	200	mV
Quiescent Current	I_{IN}	Not Switching	-	-	2	mA
		Switching	-	6	-	mA
Thermal Shutdown	T_{SH}		-	150	-	°C
Supply Current Into AVDD			-	5.0	8.5	mA
Supply Current Into VGH			-	0.1	1.0	mA
VIN Stress		Pulse Width 100ms	-	-	12	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

Synchronous Current Mode Boost Regulator (V_{AVDD})

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
AVDD Output Voltage Accuracy	V_{AVDD}		–1	-	+1	%
AVDD Output Voltage Range		7Bits, Step = 0.1V	3.60	-	12.7	V
LX Oscillation Frequency	f_{OSC_AVDD}	2 Bits, Step = 200kHz	600	-	1200	kHz
		Tolerance	–20	-	+20	%
LX Current Limit	I_{LIM_LX}	1 Bits, Step = 1A Tolerance ±20%	0.8	1.0	1.2	A
			1.6	2.0	2.4	A
LX NMOS ON-Resistance	R_{ON1_NMOS}		-	0.2	0.3	Ω
LX NMOS Leakage Current	I_{Leak1_NMOS}		-	10	20	μA
LX PMOS ON-Resistance	R_{ON1_PMOS}		-	0.8	-	Ω
LX PMOS Leakage Current	I_{Leak1_PMOS}		-	1	20	μA
LX Maximum Duty Cycle	D_{MAX_LX}	V_{IN} = 2.5, V_{AVDD} = 11V, H = 0.8, f_{OSC_LX} = 1.2MHz	79.8	81.8	-	%
Line Regulation	V_{LINE_AVDD}	V_{IN} = 2.5V to 5.5V, I_{AVDD} = 200mA	-	±0.1	±0.15	%/V
Load Regulation	V_{LOAD_AVDD}	V_{IN} = 3.3V, I_{AVDD} = 20 to 200mA	–1	-	+1	%
Soft Start Time	t_{SS_AVDD}	2 Bits, Step = 20ms	20	-	80	Ms
		Tolerance	–10	-	+10	%
LX Switch ON / OFF Slew Rate	TS_{LX}	2 Bits, Step = 0.2 V/ns	0.5	-	1.1	V/ns
Over Voltage Protect Voltage	V_{OVP_AVDD}		14.5	15.0	15.5	V
		Hysteresis	1.129	1.250	1.375	V
Under Voltage Protect Voltage	V_{UVP_AVDD}		75	80	85	%
		V_{AVDD} Rising – V_{AVDD} Falling	0.5	1.5	2.5	%
Duration to UVP Trigger Time	t_{UVP_AVDD}		140	160	180	Ms
Short Circuit Protect Voltage	V_{SCP_AVDD}		25	30	35	%

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

Current Mode Boost Regulator (V_{GH})

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VGH Output Voltage Accuracy	V_{GH}		–1	-	+1	%
VGH Output Voltage Range		5 Bits, Step = 1V	10	-	37	V
VGH_LX Oscillation Frequency	f_{OSC_VGH}	1 Bits, Step = 400kHz	320	400	480	kHz
			640	800	960	kHz
VGH_LX Current Limit	I_{LIM_VGH}		1.2	1.5	1.8	A
VGH_LX NMOS ON-Resistance	R_{ON2_NMOS}		-	1.3	2.0	Ω
VGH_LX NMOS Leakage Current	I_{Leak2_NMOS}		-	10	20	μA
VGH_LX Maximum Duty Cycle	D_{MAX_VGH}	V_{AVDD} = 3.6, V_{GH} = 30V, η = 0.8, f_{OSC2} = 800kHz	88.4	90.4	-	%
Line Regulation	V_{LINE_VGH}	V_{AVDD} = 3.6 to 12.7V, I_{VGH} = 20mA	-	0.1	0.15	%/V
Load Regulation	V_{LOAD_VGH}	I_{GH} = 5 to 40mA	–1	-	+1	%
Soft Start Time	t_{SS_VGHL}	2 Bits, Step = 2ms	4	-	10	Ms
		Tolerance	–10	-	+10	%
LX Switch ON / OFF Slew Rate	TS_{VGH}	2 Bits, Step = 1.3 V/ns	2.2	-	6.0	V/ns
Over Voltage Protect Voltage	V_{OVP_VGH}		38	39	40	V
		Hysteresis	0.45	0.50	0.55	V
Under Voltage Protect Voltage	V_{UVP_VGH}		75	80	85	%
		V_{VGH} Rising – V_{VGH} Falling	0.5	1.0	1.5	%
Duration to UVP Trigger Time	t_{UVP_VGH}		140	160	180	Ms
Short Circuit Protect Voltage	V_{SCP_VGH}		25	30	35	%
VGHT Output Voltage Accuracy	V_{GHT}		–1	-	+1	%
VGHT Output Voltage Range		5 Bits, Step = 1V	10	-	37	V
VT Source Current	I_{VT}	V_{VT} = 1V	39	40	41	μA
VT Low Temperature Voltage	VT_LT		-	0.5	-	V
VT Low Temperature Voltage	VT_HT		-	1.25	-	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

Current Mode Buck Regulator (V25_BUCK)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
V25 Output Voltage Accuracy	V_{25}		–1	-	+1	%
V25 Output Voltage Range		4 Bits, Step = 0.1V	1.5	-	3.0	V
		5 Bits, Step = 0.1V	1.0	-	3.0	V
V25_LX Oscillation Frequency	f_{OSC_V25}		0.96	1.20	1.44	MHz
V25_LX Current Limit	$I_{LIM\_V25\_LX}$		1.0	1.2	1.4	A
V25_LX NMOS ON-Resistance	R_{ON3_NMOS}		-	80	100	mΩ
V25 PMOS On-Resistance	R_{ON3_PMOS}		-	250	350	mΩ
V25_LX NMOS Leakage Current	I_{Leak3_MOS}		-	10	20	μA
Line Regulation	V_{LINE_V25}	V_{IN} = 2.8 to 5.5V, I_{V25} = 200mA	-	±0.25	±0.5	%/V
Load Regulation	V_{LOAD_V25}	V_{IN} = 3.3V, I_{GH} = 1 to 400mA	–1	-	+1	%
Soft Start Time	t_{SS3}		3.2	4.0	4.8	Ms
Under Voltage Protect Voltage	V_{UVP_V25}		0.7	0.8	0.9	V
		V_{25} Rising – V_{25} Falling	100	150	200	mV
Duration to UVP Trigger Time	t_{UVP_V25}		140	160	180	Ms
Short Circuit Protect Voltage	V_{SCP_V25}		0.25	0.30	0.35	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

Low Dropout Linear Regulator (V25_LDO)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{LDOI}		2.5	-	5.5	V
Output Voltage Accuracy	V_{25}		–1%	-	+1%	V
Output Voltage Range		4 Bits, Step = 0.1V	1.5	-	3.0	V
		5 Bits, Step = 0.1V	1.0	-	3.0	V
Dropout Voltage	V_{DROP}	V_{IN} = 3.3V, I_{LDO} = 350mA	-	300	500	mV
LDO Output Current Limit	I_{LIM_LDO}		350	500	650	mA
Quiescent Current	I_{Q_LDO}		-	60	100	µA
Line Regulation	V_{LINE_LDO}	V_{IN} = 2.8 to 5.5V, V_{LDOO} = 2.5V, I_{LDO} = 150mA	-	0.1	0.3	%/V
Load Regulation	V_{LOAD_LDO}	V_{IN} = 3.3V, V_{LDOO} = 2.5V, I_{LDO} = 1 to 300mA	-	0.2	0.5	%
Under Voltage Protect Voltage	V_{UVP_LDO}		0.7	0.8	0.9	V
		V_{LDOO} Rising – V_{LDOO} Falling	100	150	200	mV
Duration to UVP Trigger Time	t_{UVP_LDO}		140	160	180	ms
Short Circuit Protect Voltage	V_{SCP_V25}		0.25	0.30	0.35	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

Negative Charge Pump Regulator (for VGL)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VGL Output Voltage Accuracy	V_{GL}		–1	-	+1	%
Output Voltage Range		6 Bits, Step = –0.1V	–8.0	-	–4.5	V
DRVN Source Current	I_{DRVN}		1	4	6	mA
Soft Start Time	t_{SS_VGHL}	2 Bits, Step = 2ms	4	-	10	ms
		Tolerance	–10	-	+10	%
Under Voltage Protect Voltage	V_{UVP_VGL}		75	80	85	%
Duration to UVP Trigger Time	t_{UVP_BUCK}		140	160	180	ms
Short Circuit Protect Voltage	V_{SCP_VGL}		25	30	35	%
Line Regulation	V_{LINE_VGL}	V_{IN} = 2.5 to 5.5V, I_{DRVN} = 0.1mA	-	1	6	mV
Effective Load Regulation Error	V_{LOAD_VGL}	V_{GL} = –8V, I_{DRVN} = 50μA to 1mA	–30	–5	-	mV

Gate Pulse Modulation (GPM)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VFLK Input Low Voltage	V_{IL_VFLK}		-	-	0.6	V
VFLK Input High Voltage	V_{IH_VFLK}		1.5	-	-	V
VFLK Input Bias Current	I_{B4}	V_{FLK} = 0 to V_{IN_LCD}	–40	-	+40	nA
Propagation Delay VFLK to VGHM	t_{PP}	V_{GH} = 20V	-	100	120	ns
VGH to VGHM Switch ON Resistance	R_{ON_SC}		10	30	50	Ω
RE to VGHM Switch ON Resistance	R_{ON_DC}		10	25	50	Ω
Delay Time (GPM)	t_{DLY}	2Bits, Step = 20ms	-	-	60	ms
Delay Time Tolerance (GPM)			–10	-	+10	%

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

RESETB

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
RESETB Output Voltage	V_{RST}	I_{RST} = 1.2mA	-	-	0.2	V
Leakage Current		V_{RST} = 2.5V	-	-	1	μA
RESETB Detect Voltage	VDIV	3Bits, Step = 0.2V	1.2	-	2.6	V
		Tolerance	–8	-	+8	%
Hysteresis	V_{HYS_DVI}		100	150	200	mV
RESETB Delay Time	t_{RST}	4 Bits, Step = 2ms	-	-	30	ms
		Tolerance	–10	-	10	%

Programmable VCOM Buffer (VCOM)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
AVDD Input Voltage Range	V_{OPPI}	AVDD–NAVDD < 18V	3.6	-	12.7	V
NAVDD Input Voltage Range	V_{OPNI}	AVDD–NAVDD < 18V	–8	-	-	V
VCOM Output Voltage Range	V_{COM}	8Bits, Step = 0.1V	–4.1	-	+5.1	V
VCOM Output Voltage Accuracy			–6		+6	LSB
VCOMT Output Voltage Range	V_{COMT}	8Bits, Step = 0.1V	–4.1	-	+5.1	V
VCOMT Output Voltage Accuracy			–6	-	+6	LSB
Load Regulation		I_{OUT} = 1 to 20mA Sourcing	-	1	2	V/A
		I_{OUT} = 1 to 20mA Sinking	-	1	2	V/A
Short Circuit Current (FAVDD Type)	I_{SHORT}	Measure I_{OP_OUT}	-	±200	-	mA
Short Circuit Current (±AVDD Type)	I_{SHORT}	Measure I_{OP_OUT}	-	±200	-	mA
Slew Rate	SR		8	12	-	V/μs
Settling Time	t_S	±0.1%, V_{OUT} = 2V step, A_V = 1, AVDD = 5V, NAVDD = –5V	-	500	-	ns
Power Supply Rejection Ratio	PSRR	Product	-	85	-	dB
Bandwidth	BW	–3dB	12	-	-	MHz
Gain- Bandwidth		Buffer Configuration	8	-	-	MHz

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

Operational Amplifier (2 OP)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
AVDD Input Voltage Range	V_{OP}	AVDD-NAVDD < 18V	3.6 0	-	12.7	V
NAVDD Input Voltage Range	V_{OP}	AVDD-NAVDD < 18V	–8	-	0	V
Input Supply Current	I_{OP}		-	3	-	mA
Input Offset Voltage	V_{OPIN}	V_{CM} = 0V	-	2	15	mV
Average Offset Voltage Drift		T_A = –40°C to +85°C	-	5	-	μV/°C
Input Bias Current	I_{B_OPIN}	V_{CM} = 0V	–40	-	+40	nA
Input Impedance	RI_N		-	1	-	GΩ
Input Capacitance	C_{IN}		-	1.35	-	pF
Input Common mode Voltage Range	V_{CM}		–5.5	-	+5.5	V
Common mode Rejection Ratio	CMRR	V_{OPIN} = –5.5V to +5.5V	50	80	-	dB
Power Supply Rejection Ratio	PSRR		60	70	-	dB
Open Loop Gain	A_{VOL}	V_{OP_OUT} = –4.5V to +4.5V	75	95	-	dB
Output Swing	V_{OP_SL}	I_{OP_OUT} = –5mA, V_{OP_IN}= –5V	-	–4.92	–4.85	V
	V_{OP_SH}	I_{OP_OUT} =+5mA, V_{OP_IN} = 5V	4.85	4.92	-	V
Continuous Output Current	I_{CONT}		-	±35	-	mA
Short Circuit Current	I_{SHORT}	Measure I_{OP_OUT}	-	±120	-	mA
Slew Rate	SR	V_{OP_OUT} = –4V to +4V, 20% to 80%	8	12	-	V/μs
Settling Time	t_S	±0.1%, V_{OUT} = 2V step, AV = 1, AVDD = 5V, NAVDD = –5V	-	500	-	ns
Bandwidth	BW	–3dB, RL = 10kΩ, CL = 10pF	-	12	-	MHz
Gain- Bandwidth Product	GBPW	RL = 10kΩ, CL = 10pF	-	5	-	MHz
Phase Margin	PM	RL = 10kΩ, CL = 10pF	-	50	-	°
Channel Seperation	CS	f = 5MHz	-	75	-	dB

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 3.3V, V_{AVDD} = 8.5V, V_{GH} = 23V, V_{GL} = -6V, V_{25} = 2.5V, NAVDD = GND)

I²C Interface

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCL, SDA Input High Voltage	V_{IH2}		1.5	-	-	V
SCL, SDA Input Low Voltage	V_{IL2}		-	-	0.6	V
SCL, SDA Input Capacitance	C_{SI}		-	5p	-	F
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA	-	-	0.4	V
SCL Clock Frequency	f_{OSCI2C}		-	-	400k	Hz
SCL Clock High Period	t_{IH3}		0.6	-	-	µs
SCL Clock Low Period	t_{IL3}		1.3	-	-	µs
SCL, SDA Receiving Rise Time	t_{R1}		-	20+0.1* C_B	300	ns
SCL, SDA Receiving Fall Time	t_{F1}		-	20+0.1* C_B	300	ns
I²C Data Setup Time	t_{S1}		100	-	-	ns
I²C Data Hold Time	t_{H1}		-	-	900	ns
I²C Setup Time for START Condition	t_{S2}		0.6	-	-	µs
I²C Hold Time for START Condition	t_{H2}		0.6	-	-	µs
I²C Bus Free Time Between STOP and START Conditions	t_{BUS}		4.7	-	-	µs
I²C Pulse Width of Suppressed Spike	t_{PS}		-	-	50	ns
I²C Bus Capacitance	C_B		-	-	400	pF
SDA, SCL Pull Up Resistor	R_{PU}		4.7	10.0	-	kΩ

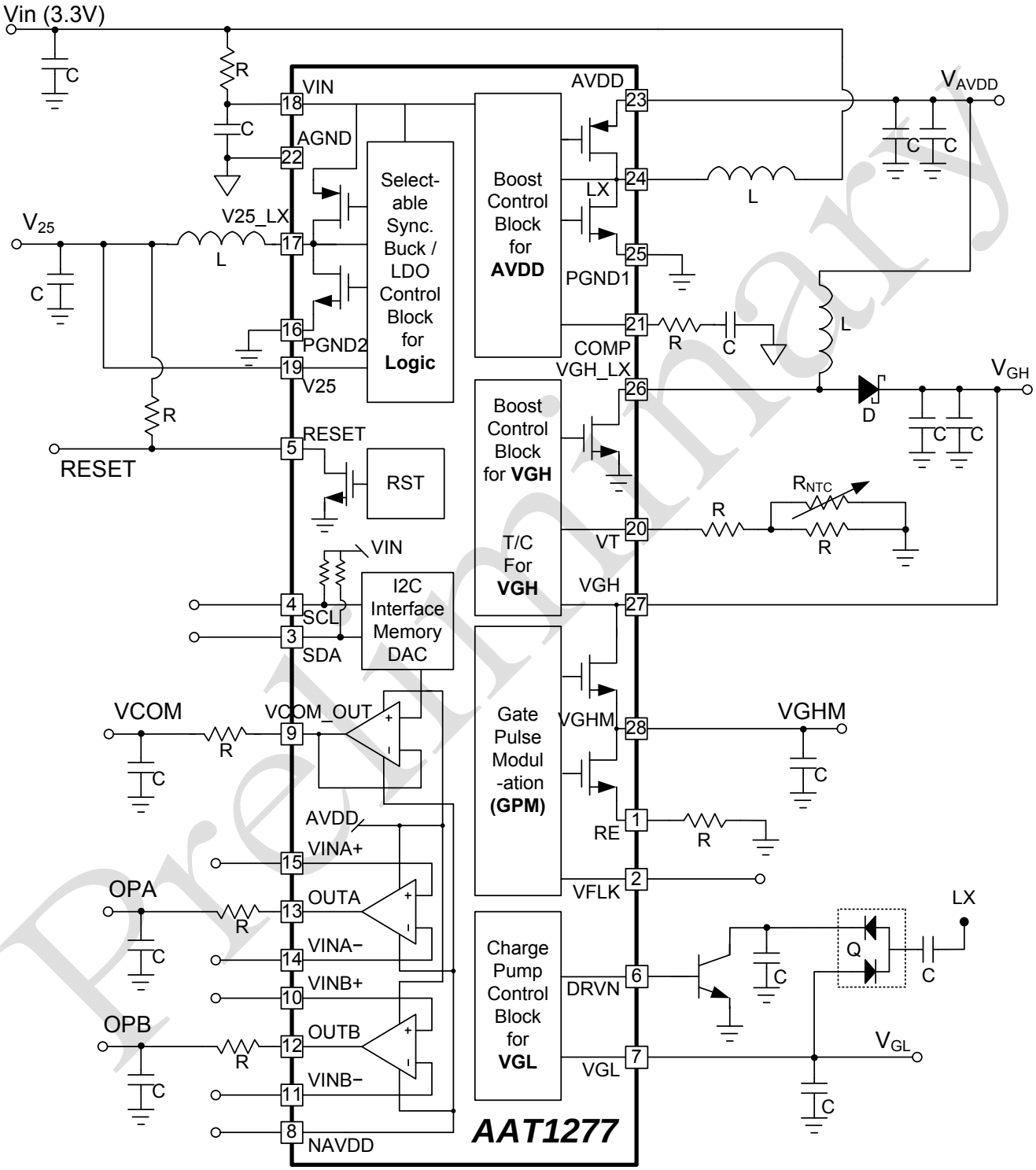
NVM

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Byte Write Time	t_{BYTE}		-	-	10	ms
Byte Read Access Time	B_{RT}		-	200	-	ns
NVM Programmable Times	N_{NVM}		-	1,000		Cycle

PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	RE	O	GPM Falling Time Setting Pin
2	VFLK	I	GPM Control Pin (High: VGHM=VGH, Low: VGHM=Discharge)
3	SDA	I	I^2C Compatible Serial Data Input/Output
4	SCL	I	I^2C Compatible Serial Clock Input
5	RESETB	O	Voltage Detector Output for Resetb
6	DRVN	O	Voltage Driver Output of Negative Charge Pump Linear Regulator
7	VGL	I	Output Sensing of Negative Charge Pump Linear Regulator
8	NAVDD	I	Negative Input of VCOM and Operational Amplifiers
9	VCOM_OUT	O	VCOM Buffer Output
10	VINB+	I	Non-Inverting Input of Operational Amplifier B
11	VINB-	I	Inverting Input of Operational Amplifier B
12	OUTB	O	Operational Amplifier B Output
13	OUTA	O	Operational Amplifier A Output
14	VINA-	I	Inverting Input of Operational Amplifier A
15	VINA+	I	Non-Inverting Input of Operational Amplifier A
16	PGND2	-	Power Ground for Buck Regulator
17	V25_LX	O	Switch Node of Buck Regulator or LDO
18	VIN	I	Power Supply Input
19	V25	I	Output Sensing of Buck Regulator or LDO
20	VT	O	Negative Temperature Compensation Pin for VGH and VCOM
21	COMP	O	Compensation Pin for AVDD Boost Regulator
22	AGND	-	Analog Ground
23	AVDD	I	Output Sensing of AVDD Boost Regulator, Positive Input of VCOM and Operational Amplifiers
24	LX	O	Switch Node of AVDD Boost Regulator
25	PGND1	-	Power Ground for VGH Regulator
26	VGH_LX	O	Switch Node of VGH_LX Boost Regulator
27	VGH	I	Output Sensing of VGH Boost Regulator
28	VGHM	O	Gate Pulse Modulation (GPM) Output
29	PGND3	-	Power Ground for AVDD Regulator

FUNCTIONAL BLOCK DIAGRAM



THEORY OF OPERATION

The AAT1277 offers a complete solution for powering TFT LCD panels. The device integrates two current mode boost regulators, one synchronous boost regulator for the source driver supply, and the second non-synchronous boost regulator with temperature compensation to generate a gate-on voltage for VGH. The AAT1277 also includes a negative charge pump linear regulator for the gate-off voltage, a synchronous buck regulator or a low dropout linear regulator alternatively for system logic power, a gate pulse modulation (GPM) for improving TFT LCD image quality, a XON reset function for input supply monitor, a unity-gain Buffer for VCOM calibrator and two operational amplifiers in the device. The device includes various system protection schemes such as soft start, power up sequencing, fault protection, and thermal shutdown. The AAT1277 also includes I^2C interface for various device settings such as output voltages, switching frequency, soft start time, delay time, etc.

Under Voltage Lockout (UVLO)

For systematic startup, AAT1277 employs a UVLO rising threshold of 2.35V typical. Thus, the input supply must exceed the UVLO threshold for the regulators to begin switching. Likewise, the device shuts down all functions when the input voltage is lower than UVLO falling threshold of 2.20V. A 150mV hysteresis is added to prevent device chattering when the input supply is noisy or unstable during power up or power down.

Boost Regulator for AVDD

The synchronous AVDD boost converter integrates a low R_{DSON} (typical 0.2Ω) NMOS for the low side switch, and a PMOS as the output rectifier. The boost output voltage, over current protection (OCP) threshold, soft start time, switching ON/OFF transient slew rate, and switching frequency are programmed via I^2C interface.

The output voltage can be set from 3.6V to 12.7V with a step resolution of 0.1V. Over current protection (OCP) threshold ranges from 1A to 2A with 1A steps, soft start time can be set from 20ms to 80ms with 20ms steps, and the LX switching ON/OFF transient slew rate can be set from 0.5V/ns to 1.1V/ns with 0.2V/ns steps. The LX switching frequency can be programmed for either 600kHz, 800kHz, 1000kHz, or 1.2MHz. The boost regulator operates from a minimum input voltage of 2.5V, and delivers an output voltage that reaches the maximum capable duty cycle. The duty cycle (D) is calculated by

$$D = \frac{V_O - V_I}{V_O} \text{ or } \frac{V_O}{V_I} = \frac{1}{1-D}$$

where V_O (V_{AVDD}) is the output of the boost regulator. Typical maximum duty cycle is approximately 80%.

At the heart of the current mode topology are two feedback loops. See the AVDD Boost Regulator Functional Block Diagram Figure 1.

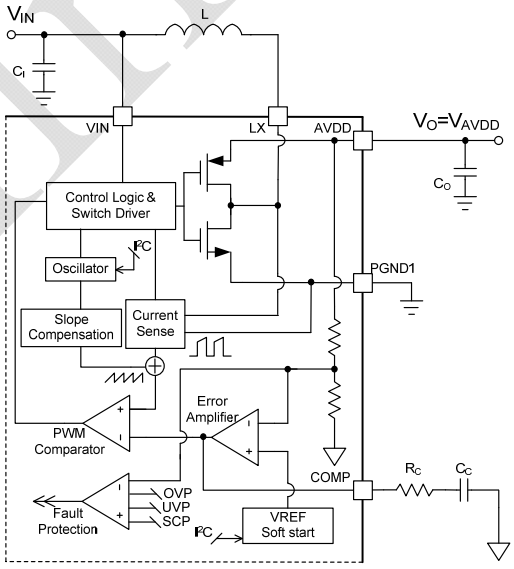


Figure 1. AVDD Boost Regulator Functional Block Diagram

One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal low side power switch. The second loop monitors the boost output via an internal feedback. This feedback voltage is compared to an internal reference voltage using a transconductance error amp. Note that the internal reference voltage is adjusted via I^2C control to set the output voltage.

Regulation is achieved by modulating the internal low

side power switch (NMOS) ON time. During the ON time, the low side NMOS is turned ON to energize the inductor while the high side power switch (PMOS) rectifier is turned OFF. When the NMOS turns off, the PMOS rectifier will turn ON, releasing the inductor energy to regulate the output. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles above 50%. During each rising edge of the internal clock pulse, the low side power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

Over Voltage Protection (OVP) for AVDD

When the AVDD boost output exceeds its Over Voltage Protection threshold (typical 15V), the AAT1277 disables the gate driver of this boost regulator and prevents the internal NMOS from switching. Once AVDD voltage falls below the OVP threshold with a hysteresis of approximately 1.25V, the boost will resume switching.

Under Voltage Protection (UVP) for AVDD

When AVDD output voltage drops below its under voltage protection threshold (80% of programmable output voltage) due to overload conditions, an internal fault timer of 160ms is activated. Once activated, if the fault condition surpasses the 160ms, the device will be shutdown. To restart the device, the V_{IN} power must be recycled below the UVLO falling threshold.

Short Circuit Protection (SCP) for AVDD

When AVDD output voltage drops below its short circuit protection threshold (30% of programmable output voltage) due to short circuit conditions, the device will immediately shutdown. This latched condition is reset by toggling V_{IN} power.

Boost Regulator for VGH

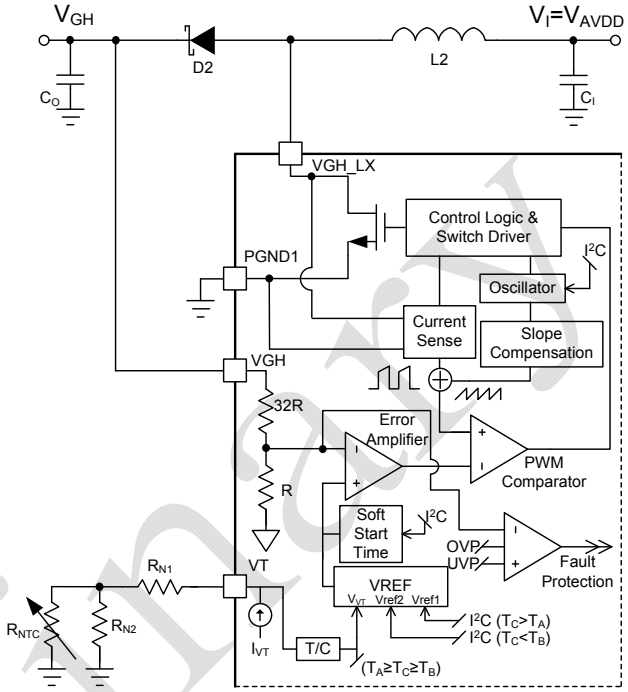


Figure 2. VGH Boost Regulator Functional Block Diagram

The non-synchronous boost regulator that supplies the VGH voltage to the TFT-LCD gate-on voltage also uses a current mode control scheme. Similarly, the output voltage is programmed via I^2C interface, and can be set from 10V to 37V with 1V step resolution. The switching frequency of the VGH boost can be set to 400kHz or 800kHz with 400kHz steps and the LX switching ON/OFF transient slew rate can be set from 2.2V/ns to 6.0V/ns with 1.3V/ns steps. The soft start time can be programmed from 4ms to 10ms using 2ms steps.

OVP & UVP for VGH

The VGH boost regulator also includes OVP and UVP. Both protection mechanisms are the same as for AVDD boost regulator, specifically 80% of VGH for UVP and typical 39V of VGH for OVP. UVP has a 160ms delay time to ensure a true UVP condition and a triggered condition latches the device, which can only be reset by recycling VIN power.

VGH Temperature Compensation

The voltage (V_{NTC}) at VT Pin will adjust the reference voltage at the non-inverting input of the error amplifier. This reference voltage will also adjust the VGH regulation voltage, and therefore tune the output voltage (V_{GH}). The output voltage (V_{GH}) is compensated accordingly. For conditions where the temperature is $T_B \leqq T_A \leqq T_C$, as show in the temperature compensation for VGH Figure 3, the reference or voltage at NTC is dependent on the voltage (V_{NTC}) at the VT Pin via the following equation:

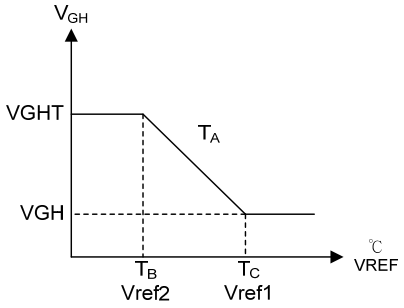


Figure 3. Temperature Compensation for VGH

$$V_{NTC} = I_{NTC} \times \left(R_{N2} + \frac{R_{N1} + R_{NTC}}{R_{N1} \times R_{NTC}} \right)$$

Thus, the output voltage V_{GH} will be

$$V_{GH} = k \times V_{NTC}$$

where k =33 is the internal resistive voltage divider ratio at the non-inverting input of the error amplifier,

If the ambient temperature T_A is below T_B, the V_{GH} voltage will be VGHT, which is set via I^2C and can be set from 25V to 39V with a 1V resolution. Likewise, if T_A is above T_C, the reference generated will be Vref1, and the V_{GH} voltage will be again dependent on the I^2C setting for a range of 15V to 35V. The conditions and equations that determine the V_{GH} voltage are summarized in Table 1.

Table 1.

°C / V	$T_A < T_B$	$T_B \leqq T_A \leqq T_C$	$T_A > T_C$
VREF	Vref2	V_{VT}	Vref1
VGH	VGHT, I^2C Setting	Dependent on external R_{NTC} network	VGH, I^2C Setting

V25 Voltage Selection

The V25 Voltage could be supplied either by the Buck regulator, or LDO determined by the state of BUCK or LDO configuration bit in the CONFIG register.

Buck Regulator for V25

The buck regulator includes a high-side PMOS and a low-side NMOS which eliminate the need for an external Schottky diode. Low on-resistance for both the switches maximizes efficiency. Moreover, the buck is compensated internally so that no external compensation network is required.

The buck output voltage is programmed via I^2C interface, and can be set from 1.5V to 3.0V with 0.1V step resolution. It operates at a fixed switching frequency of 1.2MHz and build in 4ms soft start time.

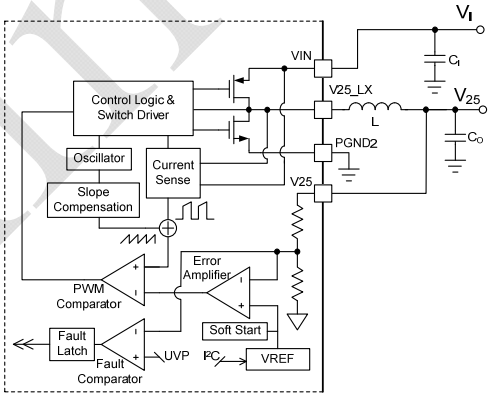


Figure 3. V25 Buck Regulator Functional Block Diagram

The buck regulator also uses the peak current mode PWM control scheme for fast transient response and cycle-by-cycle current limiting. The PWM maintains a constant frequency and varies the duty ratio according to the output voltage and load current. This modulation scheme provides high efficiency at medium to heavy load conditions, and reduces the output ripple at light load conditions. It regulates output voltage from V_{IN} down to an output voltage as low as 1.5V (1.0V). The duty cycle D is calculated by

$$D = \frac{V_O}{V_I} \quad (V_O = V_{25})$$

where V_O (V_{25}) is the output voltage of the buck regulator.

Buck Current Limit

The buck regulator includes cycle by cycle current limiting, with a threshold of typically 1.2A. When the current limit threshold is reached, the high side PMOS switch is turned off, releasing the inductive energy.

LDO for V25

The integrated LDO output voltage can be programmed form 1.5V to 3.0V via V25 register and the LDO starts as soon as the supply voltage exceeds the UVLO threshold with 4ms soft-start time, the same time as the buck regulator. The LDO is capable of a minimum 350mA output load.

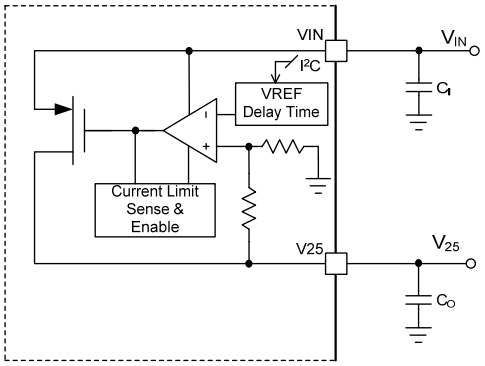


Figure4. V25 LDO Function Block Diagram

UVP for V25

The Buck regulator also includes UVP protection mechanisms. When the buck output drops below the Under Voltage Protection threshold (typical 0.8V), an internal fault timer counter is activated. Once the fault condition surpasses 160ms, the buck and other regulators will be shutdown. To restart the device, the VIN power must be recycled below the UVLO falling threshold.

Negative Charge Pump Linear Regulator for VGL

The AAT1277 integrates a Charge pump controller which drives an external NPN pass transistor to form a linear regulator that receives an input voltage provided by the charge pump, and generates a linear negative supply for the TFT LCD panel gate-off voltage. For the linear regulator to deliver the required output voltage and current, an base-to-emitter resistance (6.8kΩ) for external NPN pass transistor guarantes a base-drive current. The maximum output voltage capability is determined by the number of charge pump stage, but the actual regulated output voltage is set via I^2C interface. Using a 6 bit resolution, the VGL voltage can be set from –8.0V to –4.5V with 0.1 steps. Typical application uses a single stage, as shown in Figure 5.

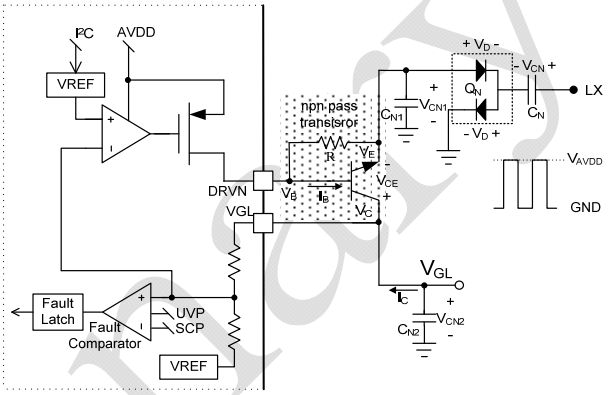


Figure 5. Negative Charge Pump Linear Regulator Functional Block Diagram

When the LX is High (V_{AVDD}), the flying capacitor C_N will charge as the lower diode will turn on and create a path to ground, and $V_{CN}+V_D=V_{AVDD}$. When the LX is Low (GND), the flying capacitor C_N is level shifted in the negative direction, and the node connecting between C_N and Q_N becomes ($-V_{CN}$). Thus, charge will flow from the output C_{N2} to C_N by through the external NPN pass transistor, and the output can be expressed as

$(-V_{CN})=V_{CN2}-V_{CE}-V_D \rightarrow V_{CN2}=(-V_{CN})+V_{CE}+V_D$

$V_{CN2}=(-V_{AVDD})+2V_D+V_{CE}$

The voltage magnitude of V_{CE} is controlled by the drive strength of DRVN, which is a p-channel open-drain output. When the NPN pass transistor is fully turned ON, the maximum capable output of this single stage charge pump is approximately

$V_{GL}=V_{CN2}=(-V_{AVDD})+0.8V$

where $V_{CE}\approx0.2V$, $V_D\approx0.3V$.

NPN PASS Transistor

For the linear regulator to deliver the required output voltage and current, the NPN transistor must be properly selected. The transistor's current gain (h_{FE}) limits the guaranteed maximum output current I_C to:

$$I_C = h_{FE} \times (I_B - \frac{V_{BE}}{R_{BE}})$$

where I_B is the base current, V_{BE} is the bass-to-emitter forward voltage drop, and R_{BE} is the pull-up resistor connected between the transistor's base and emitter. Note that too high of a transistor current gain can destabilize the linear regulator output due to a high loop gain. For the AAT1277, the bias current of the negative linear regulator controller is 0.1mA, therefore, the base-to-emitter resistor should be

$$R_{BE} = \frac{V_{BE}}{0.1mA} = \frac{0.7V}{0.1mA} \gg 6.8k\Omega$$

This should provide an output current of at least 50mA. Other factors such as the transistor saturation voltage at maximum output load current and maximum power dissipation rating of the transistor must be considered when selecting the proper NPN pass transistor.

Charge Pump Flying Capacitors

Use a 0.1µF ~ 0.47µF for the flying capacitor (C_N) and make sure that the voltage rating (V_{CN}) of the capacitor is adequate per the number of stages. The voltage rating of the capacitor must satisfy

$V_{CN} > n \times V_{AVDD}$

Where V_{AVDD} is the input supply to the charge pumps, and n is the number of stages per charge pump. Note that the negative charge pump uses 1 stage, i.e. n = 1.

Output Capacitor

The output capacitor of the linear regulator affects the stability of the regulator. To ensure stability, choose an output capacitor in the range of 1µF ~ 4.7µF, with low ESR.

Gate Pulse Modulation (GPM)

An internal high voltage switch controller is included for gate pulse modulation which provides gate shaping to improve image quality in TFT LCD applications. The circuitry consist of two high voltage PMOS, one between VGH and VGHM, and another between VGHM and RE. See Figure 6 for the Gate Pulse Modulation Functional Block Diagram.

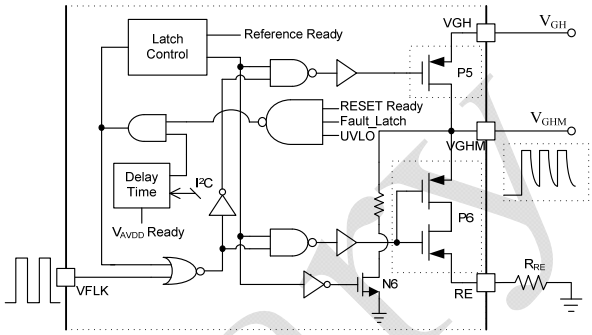


Figure 6. Gate Pulse Modulation Functional Block Diagram

When the switch controller is enabled, logic level on the VFLK input will determine which PMOS switch is ON or OFF. If VFLK is logic High, P5 turns on and P6 turns off, VGHM connects to VGH. If VFLK is logic Low, P5 turns off and P6 turns on, VGHM connects to RE, and the VGHM output (V_{GHM}) is discharged via the resistor connected at RE to ground. Note that the resistor (R_{RE}) value can be adjusted to different discharge time or high to low transient slope rate.

The GPM is enabled only after a set of power ready condition is present. For the GPM to be enabled, the device supply voltage should exceed the UVLO threshold, RESET function must be power on ready, no fault condition is present, and the programmable delayed time, t_{DLY} range from 0ms to 80ms with 20ms step resolution, should have passed after V_{GH} soft start has completed. Note that during the GPM enable period, VGH output will be internally pulled to ground via an internal resistor and NMOS (N6). Once enabled, VFLK input will control the internal switches.

During operation, if the input supply falls below the UVLO threshold, the GPM will be immediately disabled. Instantly, the high side PMOS P5 will turn on, the low side PMOS P6 will turn off simultaneously, and VFLK input will have no control over the PMOS switches.

RESETB (XAO)

This device has an internal reset circuit to monitor the voltage at V25. When V25 is lower than the detect threshold VDIV, RESET output will be pulled low. RESETB is an open-drain output that needs a pull-up resistor (R_X = 10kΩ) to a system supply. The VDIV is set via I^2C from 1.2V to 2.6V with 0.2V step resolution. In typical application, see Figure 7 for RESETB Functional Block Diagram.

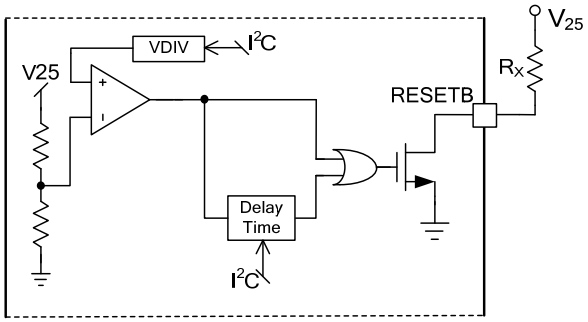


Figure 7. RESETB Functional Block Diagram

When V25 rises above its UVLO threshold (2.35V typ.), V_{HYS_DIVI}, after V25 had finished ramp, the output will be pulled High after t_{RST} delay time has completed. The t_{RST} delay time ranges from 0ms to 30ms with 2ms step resolution and also can be set via I^2C. See Figure 8 for RESETB Operation Timing Chart

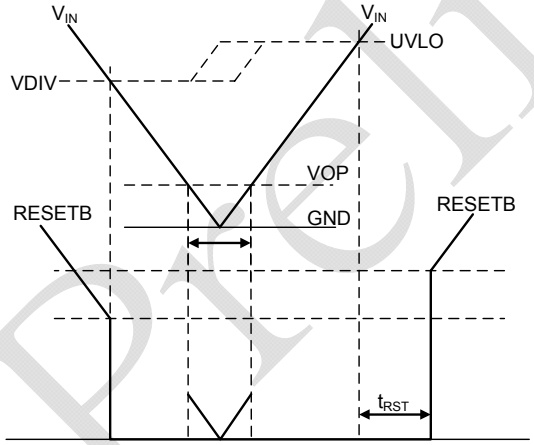


Figure 8. RESETB Operation Timing Chart

Programmable VCOM Buffer

The I^2C programmable VCOM operation amplifier can be used to digitally adjust a panel's VCOM voltage to remove flicker.

The VCOM voltage calibration needs two steps for adjustment. First step is to set the central value of VCOM voltage according to the V_{AVDD}, V_{GH}, and LCD panel characteristic. The VCOM voltage is programmable from 0.8V to 5.1V or -4.1V to +0.2V by VCOM register. The first step is normally done in PCB assembly manufacture.

Second step is to calibrate the VCOM voltage on the LCD panel assembly line by VCOM RAM register through I^2C digital interface. The VCOM register value indicates the voltage increment or decrement of VCOM_OUT which is preset by V_{COM}. Once the proper value is identified, the V_{COM} register value can be renewed with VCOM register value added. The default value for VCOM register is 1,000,000. If 100,0001 is written into VCOM register, the V_{COM} value will increase with one DAC step. In the other hand if 0111,111 is written to VCOM register, the V_{COM} will decrease with one DAC step.

The VCOM voltage also supports temperature compensation and allows its output voltage to transition from a lower voltage at low temperatures V_{COMT} to a higher voltage at high temperatures V_{COM}. The output voltage with temperature compensation is decided by voltage at the VT pin. The thermistor network formed by R1, R2, and RNTC generates a voltage at the VT pin whose value decreases with increasing temperature. With proper selection of the external components RNTC, R1, and R2, temperatures THOT and TCOLD can be configured to suit each display's characteristics. The temperature compensation resolution is 6 Bits. The temperature compensation for VCOM could be turn on/off by bit VCOMT in register CONFIG. If temperature compensation for VCOM is ON state, both V_{COM} and V_{COMT} need to be input. Otherwise only V_{COM} is active for VCOM voltage setting without temperature compensation.

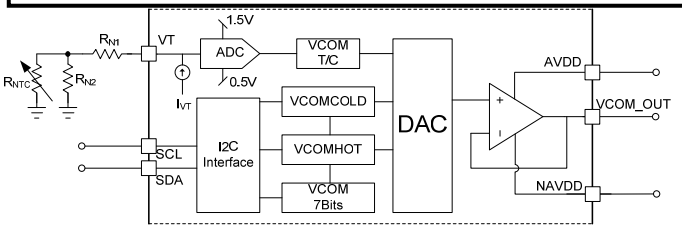


Figure 9. PVCOM Function Block

Operational Amplifiers

There are two operational amplifiers in the device. Both of them are capable of rail-to-rail input and output, ±120mA output short-circuit current, and a 12V/μs slew rate. The positive and negative supplies of operational amplifiers are connected to the AVDD pin and NAVDD pin individually. For minimize the power consumption, setting the OPA_A bit or OPA_B bit in CONFIG register can turn on or off operational amplifier individually.

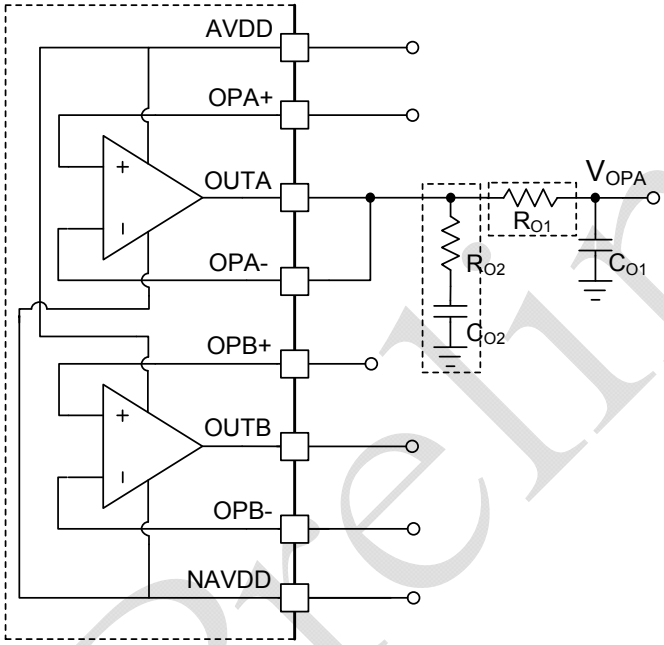


Figure 10. Operational Amplifier Functional Block Diagram

In the unity-gain configuration, the capacitive load adds a pole to the loop gain that impacts the stability of the system and leads to output peaking, ringing and oscillation. A higher pole frequency results in greater stability. In fact, if the pole frequency is lower than or close to the unity gain frequency, the pole can have a significant negative impact on phase and gain margins. Therefore, the stability decreases when the capacitive load increases.

One method of improving capacitive load drive is to insert a 2Ω to 20Ω resistor (R_{O1}) in series with the output, as shown in Figure 6. This reduces ringing with large capacitive loads while maintaining DC accuracy.

Another method for improving transient response is to add a snubber circuit at the output. A snubber circuit consists of a resistor (R_{O2}) in series with a capacitor (C_{O2}), which improves output settling time and reduces peaking. The advantage of this topology is that it draws no DC current nor does it reduce the gain.

Thermal Shutdown

The AAT1277 device enters into fault protection shutdown when the junction temperature reaches approximately 150°C. To restart the device when the junction temperature has fallen below the thermal shutdown threshold, recycle the device supply power below the UVLO falling threshold.

Power On/Off Sequence

The AAT1277 Power On/Off Sequence is as shown in Figure 11 and Figure 12.

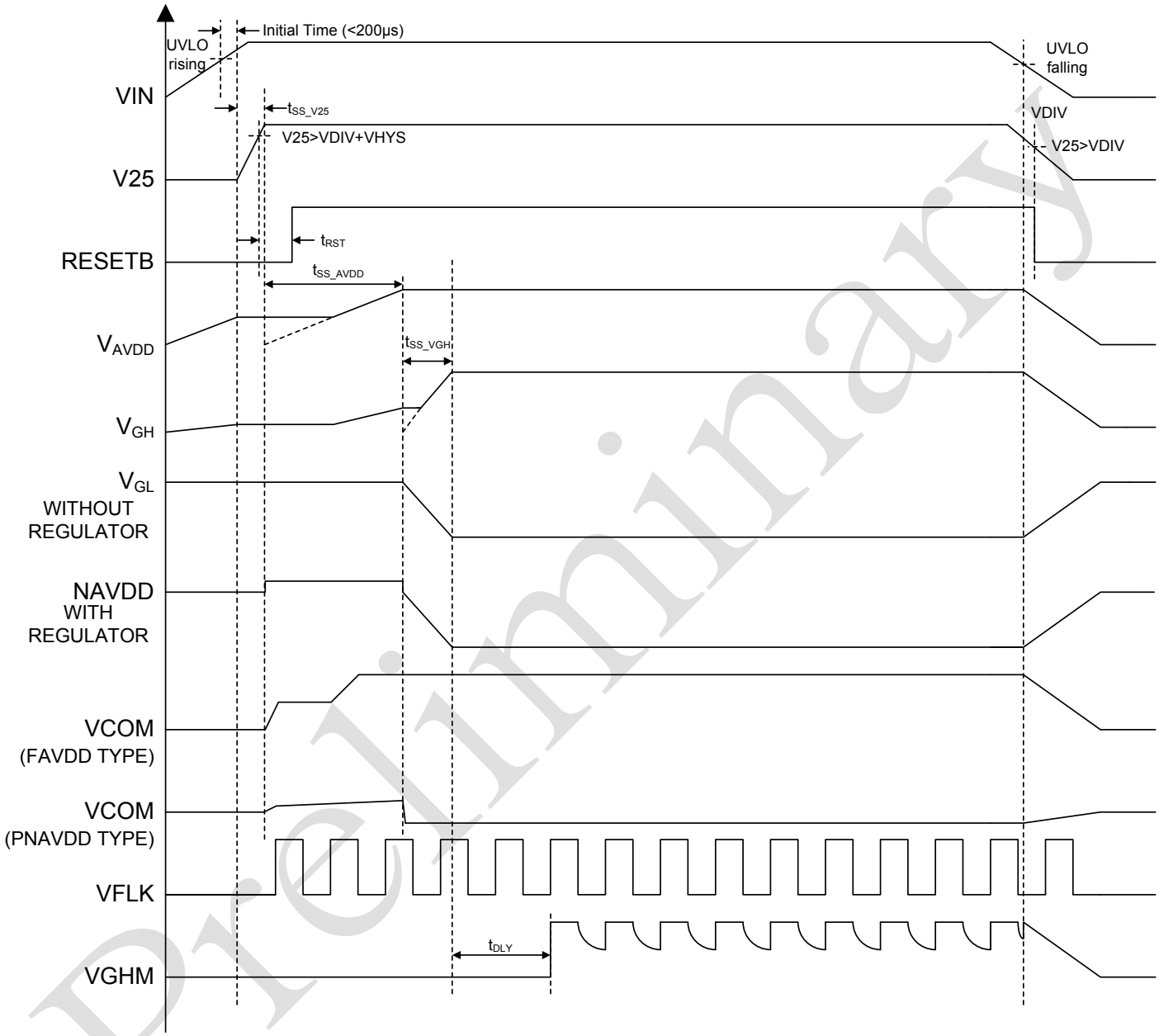


Figure 11. Power On/Off Sequence Timing Diagram (UVLO>VDIV)

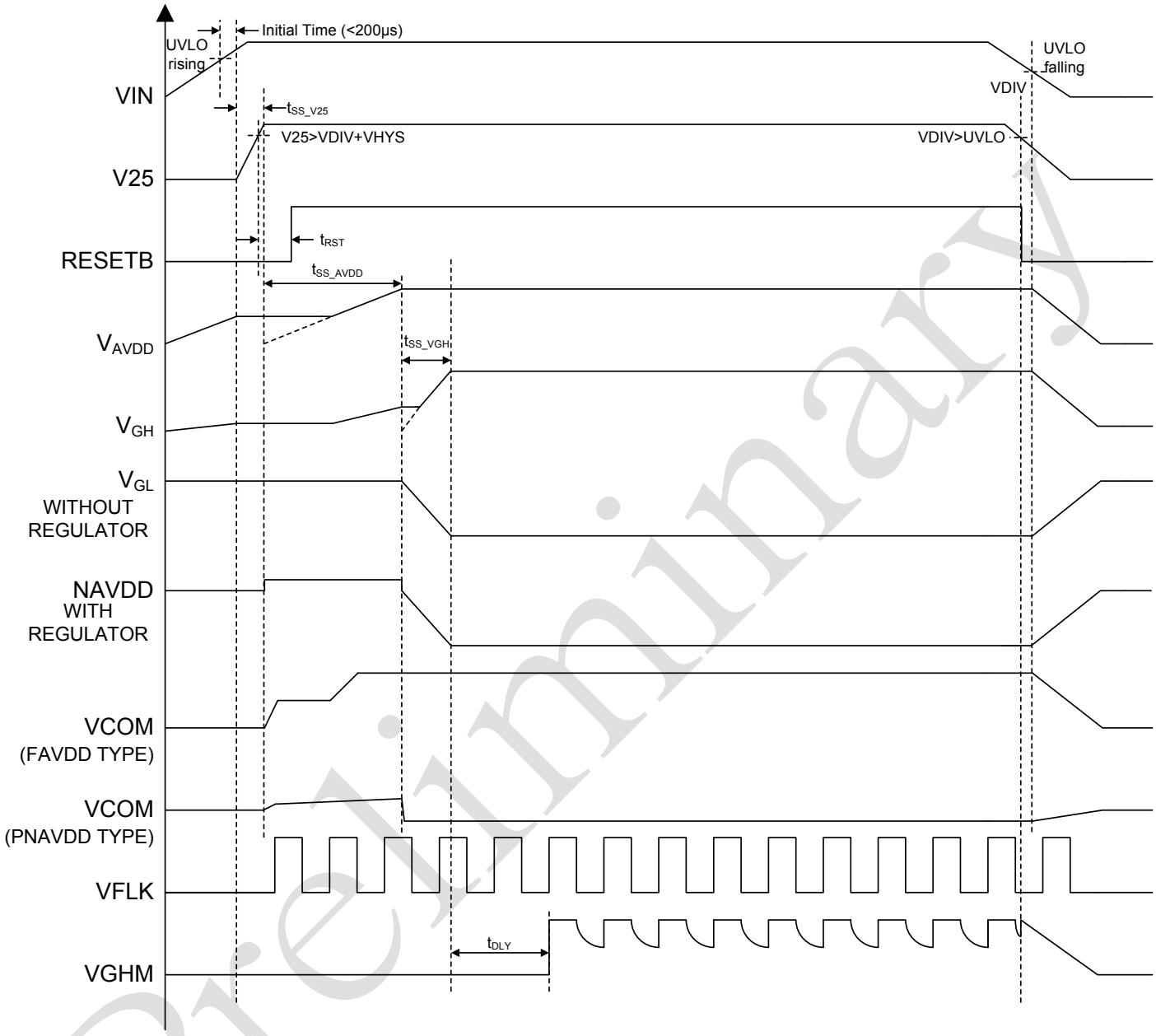


Figure 12. Power On/Off Sequence Timing Diagram (VDIV>UVLO)

I²C Serial Interface

The AAT1277 features an I²C-compatible, 2-wire serial interface consisting of a SDA and a SCL. SDA and SCL are an I/O with an open-drain output that requires a pull up resistor to realize high-logic levels. Pull up resistor values should be chosen to ensure that the rise and fall times are within specification. A typical value for the pull up resistors is 4.7kΩ. Each slave on the I²C bus responds to a slave address byte sent immediately following a Start Condition. Below diagram shows the definition of timing on I²C bus:

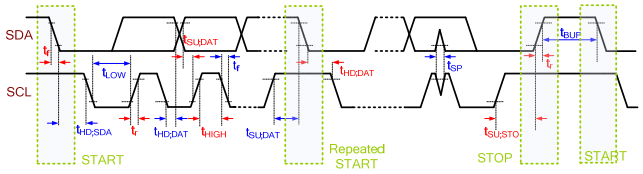


Figure 13. Definition of timing on I²C bus

The slave address byte contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit. The AAT1277 consist of two slave addresses, one slave address for accessing the PVCOM, the other slave address for accessing the PMIC section (Power Management Integrated Circuit). Below diagram shows the two slave addresses:

Table 3. PVCOM Slave Address byte

1	0	0	1	1	1	1	R/W
MSB							LSB

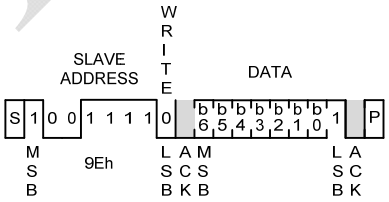
Table 4 PMIC Slave Address byte

1	1	1	0	1	0	0	R/W
MSB							LSB

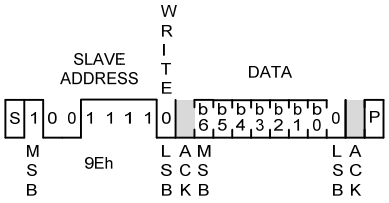
I²C Protocol for PVCOM

When the R/W bit is 0 (such as in 9Eh), the master is indicating it will write data to the slave. If R/W = 1 (9Fh in this case), the master is indicating it wants to read from the slave. During an I2C write operation, the master must transmit a register address to identify the memory location where the slave is to store the data.

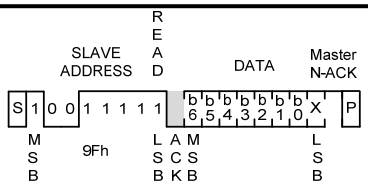
A master device writes data to DR (DAC Register) by the following timing diagram.



A master device writes data to DR (DAC Register) and EE (EEPROM) by the following timing diagram.



A master reading data from EE by the following timing diagram: (then DR = EE)



S: Start Condition, P: Stop Condition, X : Don't Care.

: Master to Slave, :Slave to Master

I²C Protocol for PMIC

When the R/W bit is 0 (such as in E8h), the master is indicating it will write data to the slave. If R/W = 1 (E9h in this case), the master is indicating it wants to read from the slave. During an I2C write operation, the master must transmit a register address to identify the memory location where the slave is to store the data. The register address is always the second byte transmitted during a write operation following the slave address byte. The AAT1277 PMIC register addresses refer to the I2C register map.

During power-up, the values stored in the EE (EEPROM, nonvolatile memory) are recalled into the DR (DAC Register, volatile memory).

WRITE OPERATION

Write Single Byte To DR (DAC Register):

Step 1: Master sends Start Condition.

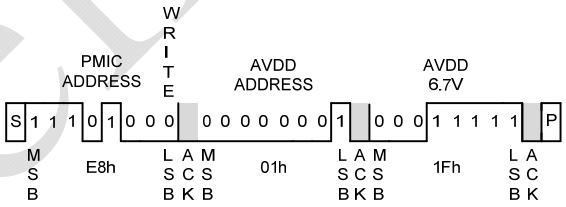
Step 2: Master sends the value E8h. (the AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 3: Send DR address (ex.01h, address of AVDD)
AAT1277 will acknowledge a bit for this byte.

Step 4: Send the data to be written to the DR (ex.1Fh, VCC = 6.7V) AAT1277 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Example: Writing 1Fh (6.7V) to the DR address 01h (AVDD)



Write Multiple Bytes To DR (DAC Register):

Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

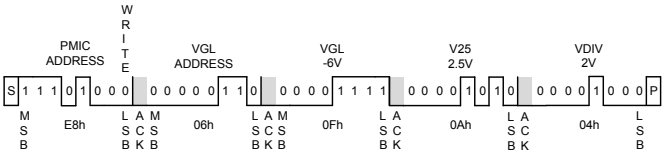
Step 3: Send DR address (ex.06h, address of VGL)
AAT1277 will acknowledge a bit for this byte.

Step 4: Send the data to be written to the DR (ex.0Fh, VGL=-6V) AAT1277 will acknowledge a bit for this byte.

Step 5: Master continues sending the other bytes to be written to the DRs. AAT1277 will acknowledge a bit for each byte and DR address will automatically increase.

Step 6: Master sends Stop Condition.

Example: Writing 0Fh(-6V), 0Ah(2.5V), 04h(2V) to the DR address 06h, 07h, 08h (VGL, V25, VDIV)



Write All DR (DAC Register) Data To EE (EEPROM):

Step 1: Master sends Start Condition.

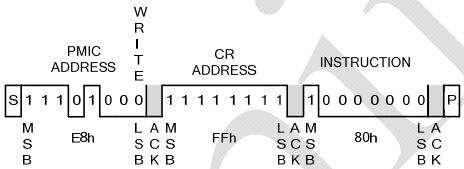
Step 2: Master sends the value E8h. (the AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 3: Send CR (Control Register) address (FFh)
AAT1277 will acknowledge a bit for this byte.

Step 4: Send the instruction 10000000b (X: Don't care, ex. 80h) to make duplicate data from DR to EE. AAT1277 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Example: Writing all DR data to EE.



READ OPERATION

Read Single Data From DAC Register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (the AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1277 will acknowledge a bit for this byte.

Step 4: Send the instruction 00000000b (X: Don't care, ex. 00h) to specify that the data is read from the DR. AAT1277 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.05h, address of AVDD) AAT1277 will acknowledge a bit for this byte.

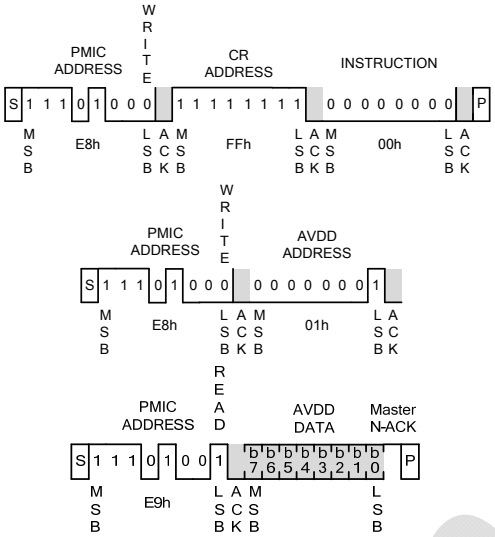
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value E9h. (the AAT1277 PMIC address 1110100b and R/W bit = High)
AAT1277 will acknowledge a bit for this byte.

Step 11: Master read the data from DR and not-acknowledges for this byte.

Step 12: Master sends Stop Condition.

Example: Reading data from the DR addresses 01h (AVDD)



Read Multiple Data From DAC Register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1277 will acknowledge a bit for this byte.

Step 4: Send the instruction 0XXXXXX0b (X: Don't care, ex. 00h) to specify that the data is read from the DR. AAT1277 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.05h, address of AVDD) AAT1277 will acknowledge a bit for this byte.

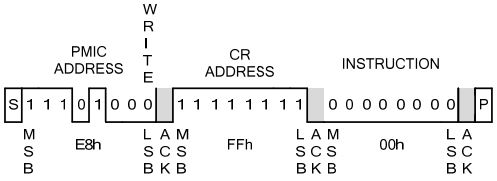
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

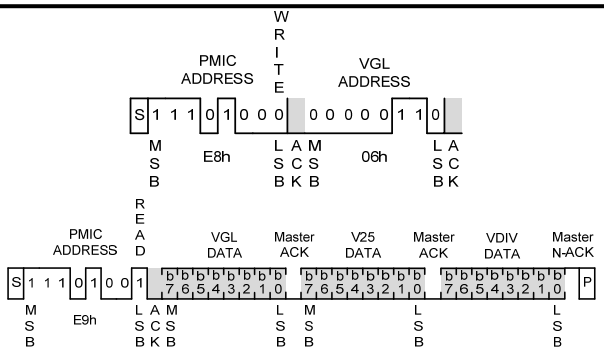
Step 10: Master sends the value E9h. (The AAT1277 PMIC address 1110100b and R/W bit = High)
AAT1277 will acknowledge a bit for this byte.

Step 11: Master continues read the data from DR and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The DR address will automatically increase.

Step 12: Master sends Stop Condition.

Example: Reading data from the DR addresses 06h, 07h, 08h (VGL, V25, VDIV)





Read Single Data From EEPROM (EE):

Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1277 will acknowledge a bit for this byte.

Step 4: Send the instruction 0XXXXXX1b (X: Don't care, ex. 01h) to specify that the data is read from the EE.
AAT1277 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 8: Send specified EE address to be read (ex.01h, address of AVDD) AAT1277 will acknowledge a bit for this byte.

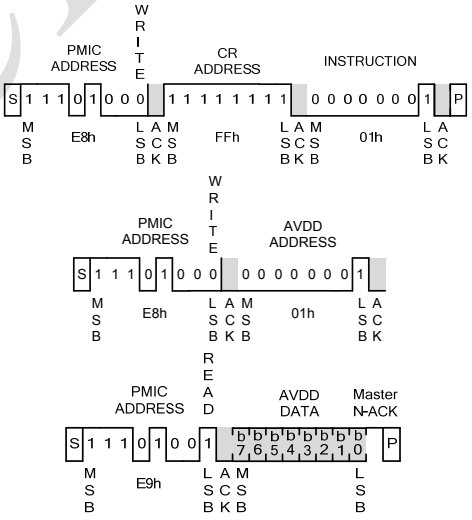
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value E9h. (The AAT1277 PMIC address 1110100b and R/W bit = High)
AAT1277 will acknowledge a bit for this byte.

Step 11: Master read the data from EE and not-acknowledges for this byte.

Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses 01h (AVDD)



Read Multiple Data From EEPROM (EE):

Step 1: Master sends Start Condition.

Step 2: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low) AAT1277 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1277 will acknowledge a bit for this byte

Step 4: Send the instruction 0XXXXXX1b (X: Don't care, ex. 01h) to specify that the data is read from the EE. AAT1277 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value E8h. (The AAT1277 PMIC address 1110100b and R/W bit = Low)
AAT1277 will acknowledge a bit for this byte.

Step 8: Send specified EE address to be read (ex.03h, address of AVDD) AAT1277 will acknowledge a bit for this byte.

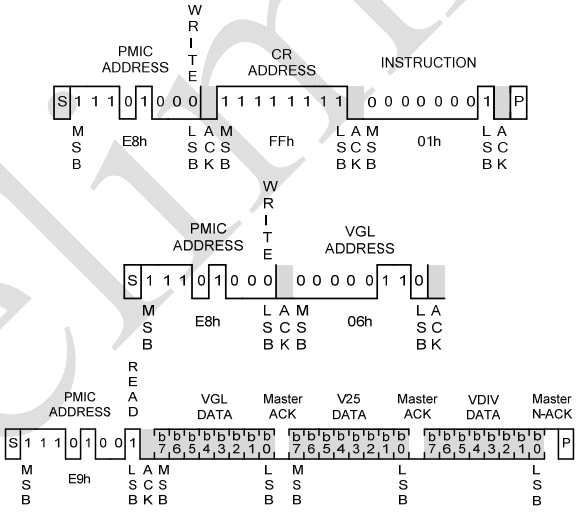
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value E9h. (The AAT1277 PMIC address 1110100b and R/W bit = High)
AAT1277 will acknowledge a bit for this byte.

Step 11: Master continues read the data from EE and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The EE address will automatically increase.

Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses 06h, 07h, 08h (VGL, V25, VDIV)



S: Start Condition, P: Stop Condition, X: Don't Care.

: Master to Slave, :Slave to Master

PMIC I2C INTERFACE REGISTER DESCRIPTION

REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
00h	CONFIG	73h	Sets function control bits
01h	AVDD	31h	Sets the output voltage of AVDD boost converter
02h	AVDDCONFIG	4Fh	Sets miscellaneous configuration bits for AVDD boost converter
03h	VGH	0Dh	Sets the output voltage of VGH boost converter at high temperatures (VGHT = 0) or VGH boost converter (VGHT=1)
04h	VGHT	14h	Sets the output voltage of VGH boost converter at low temperatures (VGHT=0)
05h	VGHCONFIG	03h	Sets miscellaneous configuration bits for VGH boost converte
06h	VGL	0Fh	Sets the output voltage of VGL linear regulator
07h	V25	0Ah	Sets the output voltage of buck converter
08h	VDIV	04h	Sets the threshold of the /RST signals
09h	RESETB	06h	Sets the resetb pulse duration
0Ah	DLY	01h	Sets the gate voltage shaping delay
0Bh	VCOM	57h	Presets the output voltage of VCOM reference at high temperatures (VCOMT = 0) or VCOM reference (VCOMT=1)
0Ch	VCOMT	52h	Presets the output voltage of VCOM reference at low temperatures (VCOMT=0)
FFh	Control	00h	Controls whether read and write operations access RAM or EEPROM registers

PMIC DAC REGISTER SETTING DESCRIPTION

CONFIG (00h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOMR	VCOMT	OPA_B	OPA_A	BUCK/LDO	VGL	VGHT	VGH

VGH	Bits	This bit enables/disables the boost converter for VGH voltage regulator.	
	0	0	Enables the VGH boot converter
		1	Disables the VGH boot converter
VGHT	Bits	This bit enables/disables the temperature compensation for VGH regulator.	
	1	0	Enables the temperature compensation for VGH voltage regulator
		1	Disables the temperature compensation for VGH voltage regulator
VGL	Bits	This bit enables/disables the VGL linear voltage regulator.	
	2	0	Enables the VGL linear voltage regulator
		1	Disables the VGL linear voltage regulator
BUCK/LDO	Bits	his bit selects the operation mode for V25 voltage regulator.	
	3	0	Selects the Buck converter for V25 voltage regulator
		1	Selects the LDO for V25 voltage regulator
OPA_A	Bits	This bit enables/disables the OPA_A operational amplifier.	
	4	0	Enables the OPA_A operational amplifier
		1	Disables the OPA_A operational amplifier
OPA_B	Bits	This bit enables/disables the OPA_B operational amplifier.	
	5	0	Enables the OPA_B operational amplifier
		1	Disables the OPA_B operational amplifier
VCOMT	Bits	This bit enables/disables the temperature compensation for VCOM voltage	
	6	0	Enables the temperature compensation for VCOM voltage
		1	Disables the temperature compensation for VCOM voltage
VCOMR	Bits	This bit select the AVDD boost current limite value	
	7	0	This bit sets the V COM voltage output range
		1	V COM = -4V~0.8V for PN AVDD Application

AVDD (01h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	V_{AVDD}						

0000000	V_{AVDD}=3.6V	0011010	V_{AVDD}=6.2V	0110100	V_{AVDD}=8.8V	1001110	V_{AVDD}=11.4V
0000001	V_{AVDD}=3.7V	0011011	V_{AVDD}=6.3V	0110101	V_{AVDD}=8.9V	1001111	V_{AVDD}=11.5V
0000010	V_{AVDD}=3.8V	0011100	V_{AVDD}=6.4V	0110110	V_{AVDD}=9.0V	1010000	V_{AVDD}=11.6V
0000011	V_{AVDD}=3.9V	0011101	V_{AVDD}=6.5V	0110111	V_{AVDD}=9.1V	1010001	V_{AVDD}=11.7V
0000100	V_{AVDD}=4.0V	0011110	V_{AVDD}=6.6V	0111000	V_{AVDD}=9.2V	1010010	V_{AVDD}=11.8V
0000101	V_{AVDD}=4.1V	0011111	V_{AVDD}=6.7V	0111001	V_{AVDD}=9.3V	1010011	V_{AVDD}=11.9V
0000110	V_{AVDD}=4.2V	0100000	V_{AVDD}=6.8V	0111010	V_{AVDD}=9.4V	1010100	V_{AVDD}=12.0V
0000111	V_{AVDD}=4.3V	0100001	V_{AVDD}=6.9V	0111011	V_{AVDD}=9.5V	1010101	V_{AVDD}=12.1V
0001000	V_{AVDD}=4.4V	0100010	V_{AVDD}=7.0V	0111100	V_{AVDD}=9.6V	1010110	V_{AVDD}=12.2V
0001001	V_{AVDD}=4.5V	0100011	V_{AVDD}=7.1V	0111101	V_{AVDD}=9.7V	1010111	V_{AVDD}=12.3V
0001010	V_{AVDD}=4.6V	0100100	V_{AVDD}=7.2V	0111110	V_{AVDD}=9.8V	1011000	V_{AVDD}=12.4V
0001011	V_{AVDD}=4.7V	0100101	V_{AVDD}=7.3V	0111111	V_{AVDD}=9.9V	1011001	V_{AVDD}=12.5V
0001100	V_{AVDD}=4.8V	0100110	V_{AVDD}=7.4V	1000000	V_{AVDD}=10.0V	1011010	V_{AVDD}=12.6V
0001101	V_{AVDD}=4.9V	0100111	V_{AVDD}=7.5V	1000001	V_{AVDD}=10.1V	1011011	V_{AVDD}=12.7V
0001110	V_{AVDD}=5.0V	0101000	V_{AVDD}=7.6V	1000010	V_{AVDD}=10.2V	Others	V_{AVDD}=12.7V
0001111	V_{AVDD}=5.1V	0101001	V_{AVDD}=7.7V	1000011	V_{AVDD}=10.3V		
0010000	V_{AVDD}=5.2V	0101010	V_{AVDD}=7.8V	1000100	V_{AVDD}=10.4V		
0010001	V_{AVDD}=5.3V	0101011	V_{AVDD}=7.9V	1000101	V_{AVDD}=10.5V		
0010010	V_{AVDD}=5.4V	0101100	V_{AVDD}=8.0V	1000110	V_{AVDD}=10.6V		
0010011	V_{AVDD}=5.5V	0101101	V_{AVDD}=8.1V	1000111	V_{AVDD}=10.7V		
0010100	V_{AVDD}=5.6V	0101110	V_{AVDD}=8.2V	1001000	V_{AVDD}=10.8V		
0010101	V_{AVDD}=5.7V	0101111	V_{AVDD}=8.3V	1001001	V_{AVDD}=10.9V		
0010110	V_{AVDD}=5.8V	0110000	V_{AVDD}=8.4V	1001010	V_{AVDD}=11.0V		
0010111	V_{AVDD}=5.9V	0110001	V_{AVDD}=8.5V	1001011	V_{AVDD}=11.1V		
0011000	V_{AVDD}=6.0V	0110010	V_{AVDD}=8.6V	1001100	V_{AVDD}=11.2V		
0011001	V_{AVDD}=6.1V	0110011	V_{AVDD}=8.7V	1001101	V_{AVDD}=11.3V		

AVDDCONFIG (02h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	I_{LIM_LX}	t_{SS_AVDD}		f_{OSC_AVDD}		TS_{LX}	

TS_{LX}	Bits	These bits configure the rising and falling speed of AVDD boost switch.	
	[1:0]	00	Tf = 0.5 V/ns Tr = 0.5 V/ns
		01	Tf = 0.7 V/ns Tr = 0.7 V/ns
		10	Tf = 0.9 V/ns Tr = 0.9 V/ns
		11	Tf = 1.1 V/ns Tr = 1.1 V/ns
f_{OSC_AVDD}	Bits	These bit configure the switching frequency of AVDD boost.	
	[3:2]	00	f_{OSC_AVDD} = 600 kHz
		01	f_{OSC_AVDD} = 800 kHz
		10	f_{OSC_AVDD} = 1000 kHz
		11	f_{OSC_AVDD} = 1200 kHz
t_{SS_AVDD}	Bits	These bits configure the soft start duration for AVDD boost regulator	
	[5:4]	00	t_{SS_AVDD} = 20 ms
		01	t_{SS_AVDD} = 40 ms
		10	t_{SS_AVDD} = 60 ms
		11	t_{SS_AVDD} = 80 ms
I_{LIM_LX}	Bits	This bit selects the AVDD boost current limit value	
	[6]	0	I_{LIM_LX} = 1A
		1	I_{LIM_LX} = 2A

VGH (03h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved			V_{GH}				

00000	V_{GH} = 10V	01111	V_{GH} = 25V
00001	V_{GH} = 11V	10000	V_{GH} = 26V
00010	V_{GH} = 12V	10001	V_{GH} = 27V
00011	V_{GH} = 13V	10010	V_{GH} = 28V
00100	V_{GH} = 14V	10011	V_{GH} = 29V
00101	V_{GH} = 15V	10100	V_{GH} = 30V
00110	V_{GH} = 16V	10101	V_{GH} = 31V
00111	V_{GH} = 17V	10110	V_{GH} = 32V
01000	V_{GH} = 18V	10111	V_{GH} = 33V
01001	V_{GH} = 19V	11000	V_{GH} = 34V
01010	V_{GH} = 20V	11001	V_{GH} = 35V
01011	V_{GH} = 21V	11010	V_{GH} = 36V
01100	V_{GH} = 22V	11011	V_{GH} = 37V
01101	V_{GH} = 23V	Others	V_{GH} = 37V
01110	V_{GH} = 24V		

VGHT (04h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved			V_{GHT}				

00000	V_{GHT} = 10V	01111	V_{GHT} = 25V
00001	V_{GHT} = 11V	10000	V_{GHT} = 26V
00010	V_{GHT} = 12V	10001	V_{GHT} = 27V
00011	V_{GHT} = 13V	10010	V_{GHT} = 28V
00100	V_{GHT} = 14V	10011	V_{GHT} = 29V
00101	V_{GHT} = 15V	10100	V_{GHT} = 30V
00110	V_{GHT} = 16V	10101	V_{GHT} = 31V
00111	V_{GHT} = 17V	10110	V_{GHT} = 32V
01000	V_{GHT} = 18V	10111	V_{GHT} = 33V
01001	V_{GHT} = 19V	11000	V_{GHT} = 34V
01010	V_{GHT} = 20V	11001	V_{GHT} = 35V
01011	V_{GHT} = 21V	11010	V_{GHT} = 36V
01100	V_{GHT} = 22V	11011	V_{GHT} = 37V
01101	V_{GHT} = 23V	Others	V_{GHT} = 37V
01110	V_{GHT} = 24V		

VGHCONFIG (05h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		VGHCONFIG					

TS_{VGH}	Bits	These bits configure the rising and falling speed of VGH boost switch.	
	[1:0]	00	Tf = 2.2 V/ns Tr = 2.25 V/ns
		01	Tf = 3.5 V/ns Tr = 3.5 V/ns
		10	Tf = 4.8 V/ns Tr = 4.8 V/ns
		11	Tf = 6.0 V/ns Tr = 6.0 V/ns
t_{SS_VGHL}	Bits	These bits configure the soft start duration for VGH boost regulator	
	[3:2]	00	t_{SS_VGHL} = 4 ms
		01	t_{SS_VGHL} = 6 ms
		10	t_{SS_VGHL} = 8 ms
		11	t_{SS_VGHL} = 10 ms
f_{OSC_VGH}	Bits	This bit select the VGH boost current limite value	
	[4]	00	f_{OSC_VGH} = 400 kHz
		01	f_{OSC_VGH} = 800 kHz

VGL (06h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		VGL					

000000	V_{GL} = -4.5V	010011	V_{GL} = -6.4V
000001	V_{GL} = -4.6V	010100	V_{GL} = -6.5V
000010	V_{GL} = -4.7V	010101	V_{GL} = -6.6V
000011	V_{GL} = -4.8V	010110	V_{GL} = -6.7V
000100	V_{GL} = -4.9V	010111	V_{GL} = -6.8V
000101	V_{GL} = -5.0V	011000	V_{GL} = -6.9V
000110	V_{GL} = -5.1V	011001	V_{GL} = -7.0V
000111	V_{GL} = -5.2V	011010	V_{GL} = -7.1V
001000	V_{GL} = -5.3V	011011	V_{GL} = -7.2V
001001	V_{GL} = -5.4V	011100	V_{GL} = -7.3V
001010	V_{GL} = -5.5V	011101	V_{GL} = -7.4V
001011	V_{GL} = -5.6V	011110	V_{GL} = -7.5V
001100	V_{GL} = -5.7V	011111	V_{GL} = -7.6V
001101	V_{GL} = -5.8V	100000	V_{GL} = -7.7V
001110	V_{GL} = -5.9V	100001	V_{GL} = -7.8V
001111	V_{GL} = -6.0V	100010	V_{GL} = -7.9V
010000	V_{GL} = -6.1V	100011	V_{GL} = -8.0V
010001	V_{GL} = -6.2V	Others	V_{GL} = -8.0V
010010	V_{GL} = -6.3V		

V25 (07h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				V_{25}			

0000	V_{25} = 1.5 V	1000	V_{25} = 2.3 V
0001	V_{25} = 1.6 V	1001	V_{25} = 2.4 V
0010	V_{25} = 1.7 V	1010	V_{25} = 2.5 V
0011	V_{25} = 1.8 V	1011	V_{25} = 2.6 V
0100	V_{25} = 1.9 V	1100	V_{25} = 2.7 V
0101	V_{25} = 2.0 V	1101	V_{25} = 2.8 V
0110	V_{25} = 2.1 V	1110	V_{25} = 2.9 V
0111	V_{25} = 2.2 V	1111	V_{25} = 3.0 V

VDIV (08h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					VDIV		

000	VDIV = 1.2 V
001	VDIV = 1.4 V
010	VDIV = 1.6 V
011	VDIV = 1.8 V
100	VDIV = 2.0 V
101	VDIV = 2.2 V
110	VDIV = 2.4 V
111	VDIV = 2.6 V

RESETB (09h)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				RESETB			

0000	t_{RST} = 0 ms	1000	t_{RST} = 16 ms
0001	t_{RST} = 2 ms	1001	t_{RST} = 18 ms
0010	t_{RST} = 4 ms	1010	t_{RST} = 20 ms
0011	t_{RST} = 6 ms	1011	t_{RST} = 22 ms
0100	t_{RST} = 8 ms	1100	t_{RST} = 24 ms
0101	t_{RST} = 10 ms	1101	t_{RST} = 26 ms
0110	t_{RST} = 12 ms	1110	t_{RST} = 28 ms
0111	t_{RST} = 14 ms	1111	t_{RST} = 30 ms

DLY (0Ah)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						DLY	

00	t_{DLY} = 0 ms
01	t_{DLY} = 20 ms
10	t_{DLY} = 40 ms
11	t_{DLY} = 60 ms

VCOM (0Bh)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
V_{COM}							

	VCOMR=0	VCOMR=1
00000000	V_{COM} = N.A.	V_{COM} = N.A.
00000001	V_{COM} = N.A.	V_{COM} = N.A.
00000010	V_{COM} = N.A.	V_{COM} = N.A.
…..	V_{COM} = N.A.	V_{COM} = N.A.
00100111	V_{COM} = N.A.	V_{COM} = N.A.
00101000	V_{COM} = 0.80V	V_{COM} = 0.20V
00101001	V_{COM} = 0.82V	V_{COM} = 0.18V
00101010	V_{COM} = 0.84V	V_{COM} = 0.16V
00101011	V_{COM} = 0.86V	V_{COM} = 0.14V
00101100	V_{COM} = 0.88V	V_{COM} = 0.12 V
……..	…….	…….
11111101	V_{COM} = 5.06V	V_{COM} = -4.06 V
11111110	V_{COM} = 5.08V	V_{COM} = -4.08 V
11111111	V_{COM} = 5.10V	V_{COM} = -4.10 V

VCOMT (0Ch)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
V_{COMT}							

	VCOMR=0	VCOMR=1
00000000	V_{COMT} = N.A.	V_{COMT} = N.A.
00000001	V_{COMT} = N.A.	V_{COMT} = N.A.
00000010	V_{COMT} = N.A.	V_{COMT} = N.A.
…..	V_{COMT} = N.A.	V_{COMT} = N.A.
00100111	V_{COMT} = N.A.	V_{COMT} = N.A.
00101000	V_{COMT} = 0.80V	V_{COMT} = 0.20V
00101001	V_{COMT} = 0.82V	V_{COMT} = 0.18V
00101010	V_{COMT} = 0.84V	V_{COMT} = 0.16V
00101011	V_{COMT} = 0.86V	V_{COMT} = 0.14V
00101100	V_{COMT} = 0.88V	V_{COMT} = 0.12 V
……..	…….	…….
11111101	V_{COMT} = 5.06V	V_{COMT} = -4.06 V
11111110	V_{COMT} = 5.08V	V_{COMT} = -4.08 V
11111111	V_{COMT} = 5.10V	V_{COMT} = -4.10 V

CONTROL (FFh)

Bit7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit0
WED	Reserved						**RED**

RED Bit [0] The state of this bit determines whether read operations return the contents of the DAC registers or the contents of the EEPROM
- 0 Read operations return the contents of the DAC registers
- 1 Read operations return the contents of the EEPROM

Reserved Bit [6:1] These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.

WED Bit [7] Setting this bit forces the contents of all DAC registers to be copied into EEPROM, thereby making them the default values during power-up. When the contents of all the DAC registers have been written to the EEPROM, the P101automatically resets this bit.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1277.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VIN pin. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VIN bypass capacitor should referenced to analog ground (AGND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost and buck regulators contain the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node LX (LX, VGH_LX, V25_LX). The input bulk capacitance should also be placed close to these power path components to shorten the power ground length between the input and output.

Feedback and Compensation Components

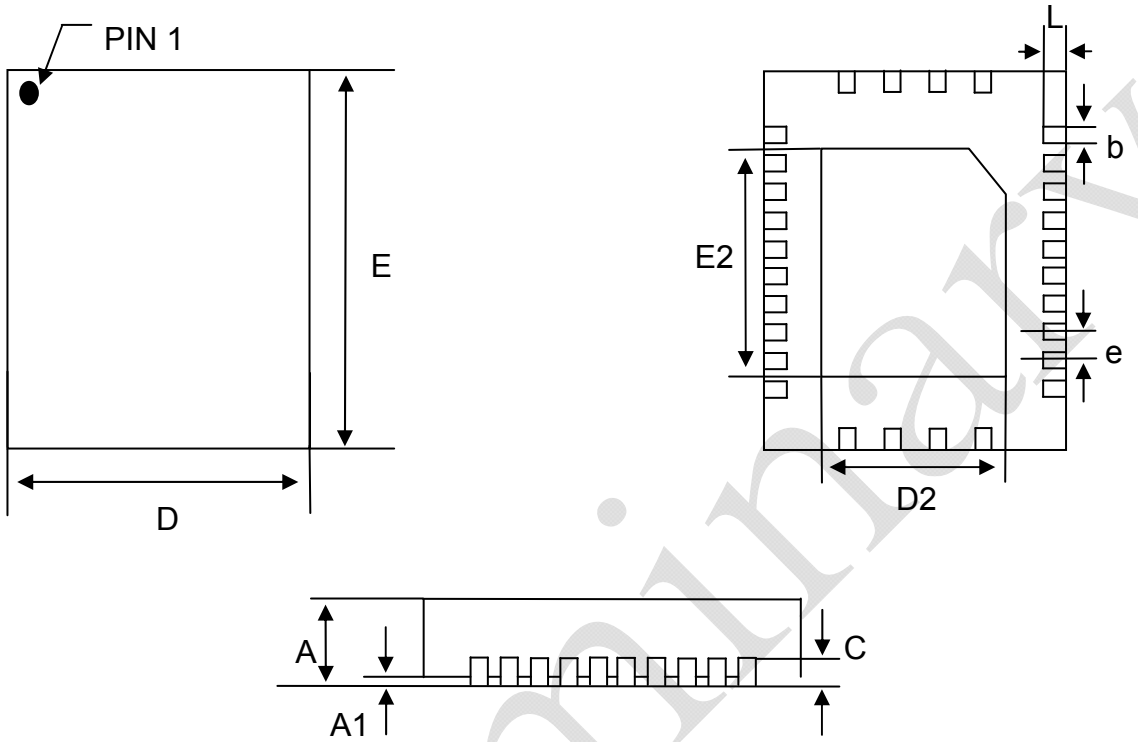
Any components for feedback should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise pickup. Likewise, compensation components should be place as close as possible to the pin or device.

Ground Plane

Use a power ground plane for the boost and buck output capacitor ground, for the boost and buck input bulk capacitor ground, charge pump output capacitor grounds, and PGND pins (PGND1, PGND2). All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create an analog ground plane (AGND) for VIN bypass capacitor grounds, compensation component ground, feedback resistive network grounds, and also the AGND pins. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (AGND) and power ground ((PGND1, PGND2) should be connected only at one signal point, near the expose pad by shorting the AGND pin to the expose pad.

PACKAGE DIMENSION

WQFN28-3.5X5.5



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
C	-----	0.20	-----
D	-----	3.50	-----
D2	1.95	2.05	2.10
E	-----	5.50	-----
E2	3.95	4.05	4.10
e	-----	0.50	-----
L	0.35	0.40	0.45