WHITE LEDS BACKLIGHT DRIVER

4-CHANNELS CURRENT BALANCING

FEATURES

- 3V to 24V Input Supply Voltage Range
- Current Mode Boost Regulator for VLED
  - Built-In 40V, 2.5A, 0.2Ω N-MOSFET
  - 500kHz~2MHz Adjustable Switching Frequency
  - Build-in Soft-Start Time
  - Adjustable OVP Voltage Level
- 4 Channel LED Current Sink Controller
  - Adjustable LED Current Up to 40mA
  - ±3% Current Accuracy
  - ±2% Current Matching
  - PWM Dimming Frequency 120Hz~30kHz
  - PWM Dimming Control
- Protection
  - Input Under-Voltage Lockout (UVLO)
  - Over Voltage Protection (OVP)
  - WLED Open Protection
  - Over Temperature Protection (OTP)
- WQFN 16-3X3X0.75 Package Available

APPLICATIONS

- Tablet LCD Panel Backlight
- Notebook LCD Panel Backlight

GENERAL DESCRIPTION

AAT1614 is a LED driver that consists of a Boost converter with a 4-channel current regulator. The device allows an input voltage range from 3V to 24V, thus suitable for applications in tablet and notebook backlight.

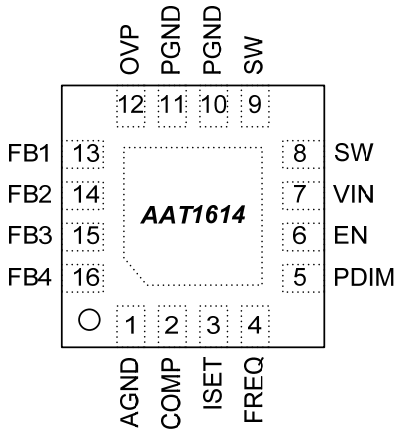
The internal current mode Boost regulator provides the LED drive voltage. This Boost integrates a 40V, 0.2Ω power NMOS which allows the converter to drive up to 40V maximum. For system optimization, the soft-start is built in to prevent output overshoots and inrushes, the switching frequency can be programmed from 500kHz to 2MHz using an external resistor and the over voltage protection threshold are also adjustable via external components.

The device includes four identical LED current sink controllers that are adjustable up to 40mA with an accuracy of ±3% by using an external resistor, and achieve a ±2% current mismatch between each channel.

The AAT1614 offers PPM (PWM to PWM) dimming control for controlling the LED brightness via external PWM dimming signal which input frequency ranges from 120Hz to 30kHz. The algorithm of PPM is that the current sink controller is turn on/off determined by the PWM input signal. The dimming algorithm includes jitter hysteresis and glitch cancellation for improved noised immunity.

The AAT1614 provides various protection mechanisms such as LED open protection, over-voltage protection, and thermal shutdown. The device is available in a small WQFN 16 pin 3x3x0.75mm with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40°C to +85°C temperature range.

PIN CONFIGURATION

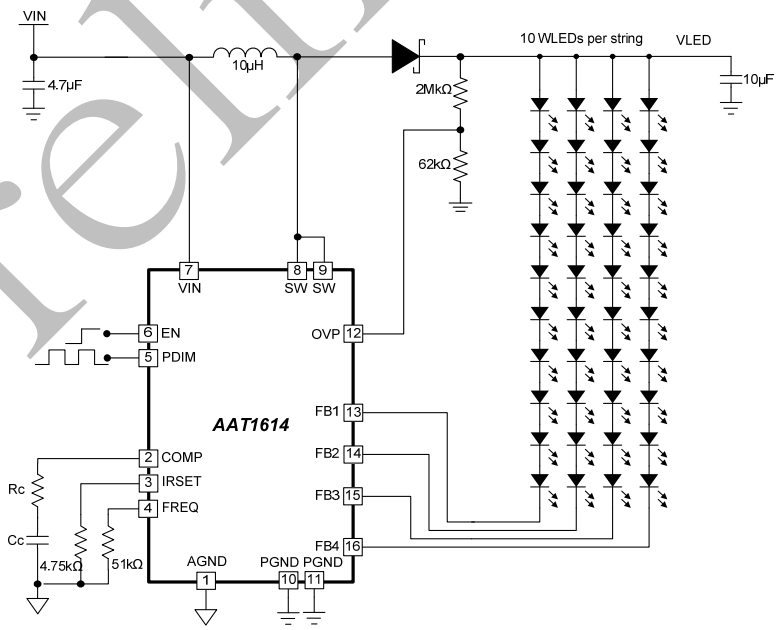


ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMPRANGE	MARKING	MARKING DESCRIPTION
AAT1614	AAT1614-Q22-T	Q22: WQFN16L -3*3	T: Tape and Reel	−40 °C to +85 °C	AAT1614 XXXXX XXXX	1. Part Name 2. Lot No. (6~9 Digits) 3. Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VIN to AGND	V_{IN}	–0.3 to +30.0	V
SW to PGND	V_{H2}	–0.3 to +45.0	V
AGND to PGND	-	–0.3 to +0.3	V
Input Voltage 1 (OVP)	V_{I1}	–0.3 to +6.0	V
Input Voltage 2 (EN, PDIM, FB1, FB2, FB3, FB4)	V_{I2}	–0.3 to +40.0	V
Output Voltage 1 (IRSET, FREQ, COMP)	V_{O1}	–0.3 to V_{IN} +6.0	V
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Impedance	θ_{JA}	47	°C / W
	θ_{JC}	2.6	
Power Dissipation @ T_A = +25°C , T_J = +125°C	P_d	2.128	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Supply Voltage	V_{IN}	3	24	V
Operating Free-Air Temperature	T_A	–40	+85	°C

ELECTRICAL CHARACTERISTICS

(VIN = EN =4.5V, f_{OSC} = 1MHz, I_{SET} = 4.75 kΩ (20mA), T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature.)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN Input Voltage Range	V_{IN}		3	-	24	V
VIN Under Voltage Lockout	V_{UVLO}	Rising (No Load)	-	2.35	-	V
		Falling (No Load)	-	2.2	-	V
Quiescent Current	I_{QN}	No Switching	-	1.0	1.5	mA
Operating Current	I_{OS}	Switching	-	3.5	4.0	mA
Shutdown Current	I_{SHDN}	EN , PDIM = GND	-	-	10	μA
EN Input Low Voltage	V_{IL}		-	-	0.6	V
EN Input High Voltage	V_{IH}		1.5	-	-	V
EN Pull Low Resistance	R_{EN}		-	350	-	kΩ
Thermal Shutdown Temperature	T_S	Rising Temperature	-	150	-	°C
Thermal Shutdown Hysteresis	T_{S_HYS}	Falling Temperature	-	40	-	°C

Boost Regulator for VLED

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SW Frequency (LOW)	f_{OSC_L}	FREQ = 120kΩ	-	500	-	kHz
SW Frequency (MEDIUM)	f_{OSC}	FREQ = 51kΩ	-	1	-	MHz
SW Frequency (HIGH)	f_{OSC_H}	FREQ = 22kΩ	-	2	-	MHz
SW NMOS On-Resistance	R_{ON}	V_{IN} = 12V, I_{SW} = 1A	-	0.2	0.5	Ω
SW Current Limit	I_{LIMT}	$3V < V_{IN} \leqq 5.5V$	1.5	2.0	-	A
		$5.5V < V_{IN} \leqq 24V$	2.0	2.5	-	A
SW Leakage Current	I_{LEAK}	V_{SW} = 40V	-	0.5	10.0	μA
SW Maximum Duty Cycle	D_{MAX}		-	92	-	%
SW Minimum On Time	T_{MIN}		-	100	-	ns
OVP Threshold Voltage	V_{OVPR}	V_{OVP} Rising	-	1.2	-	V
Voltage Gap Between VOVP and VFRD	V_{GOF}	$V_{GOF} = V_{OVP} – V_{FRD}$	-	50	-	mV

ELECTRICAL CHARACTERISTICS

(VIN = EN =4.5V, f_{OSC} = 1MHz, I_{SET} = 4.75 kΩ (20mA), T_A = –40 °C to +85 °C , unless otherwise specified. Typical values are tested at +25 °C ambient temperature.)

Current Sink Controller

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IRSET Pin Voltage	V_{IRSET}	R_{IRSET} = 4.75kΩ	-	0.6	-	V
LED Average Current	I_{LED}	R_{IRSET} = 4.75kΩ	19.4	20.0	20.6	mA
Maximum Current on Channels	I_{ROWMAX}	R_{IRSET} = 2.375kΩ	-	40	-	mA
Current Accuracy on Channels		I_{ROW} = 20mA	–3	-	+3	%
Current Mismatch on Channels		I_{ROW} = 20mA	–2	-	+2	%
Minimum FBx Regulation Voltage	V_{FB}	No LEDs Mismatch	400	450	500	mV
OPEN Detection Voltage	V_{OPEN}	V_{FB} Falling	-	50	-	mV

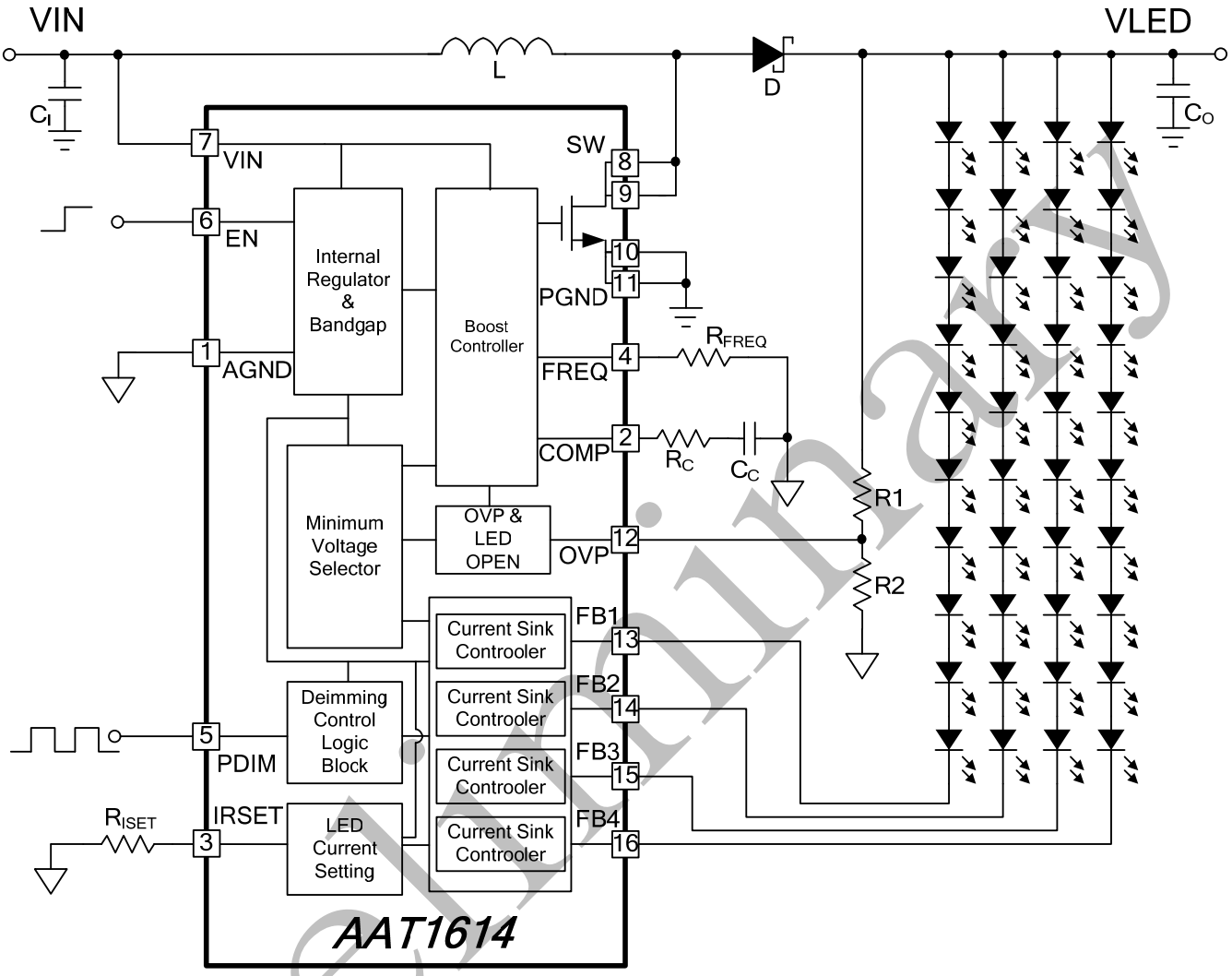
Dimming Control

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
PDIM Input Frequency Range	f_{PDIM}		120	-	30k	Hz
PDIM Input Low Voltage	V_{PDIML}		-	-	0.6	V
PDIM Input High Voltage	V_{PDIMH}		1.5	-	-	V
PDIM Pull Low Resistance	R_{PDIM}		-	500	-	kΩ

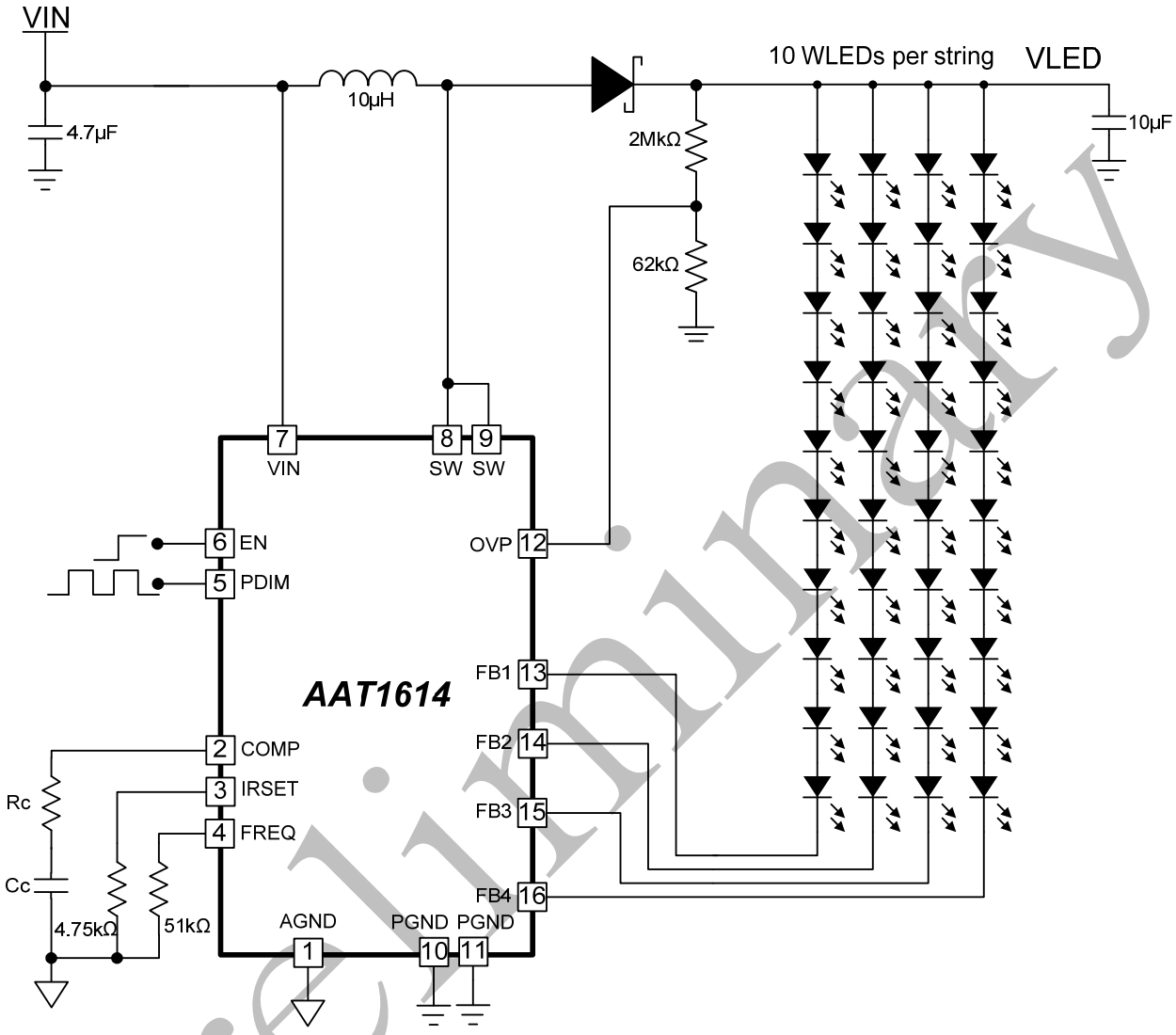
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	AGND	-	Analog GND And LED Power Return
2	COMP	O	Boost Compensation Pin
3	ISET	O	Resistor Connection for Setting LED Current
4	FREQ	O	Resistor Connection for Setting Oscillator Frequency
5	PDIM	I	PWM Brightness Control Pin
6	EN	I	Enable Pin
7	VIN	-	This Pin Is Connected to the Battery Supply
8	SW	O	Switch Pin, Drain Of the Power NMOS
9	SW	O	Switch Pin, Drain Of the Power NMOS
10	PGND	-	Power Ground (SW Power Return)
11	PGND	-	Power Ground (SW Power Return)
12	OVP	I	Over Voltage Protection Input
13	FB1	I	Constant Sink Current Pin
14	FB2	I	Constant Sink Current Pin
15	FB3	I	Constant Sink Current Pin
16	FB4	I	Constant Sink Current Pin

FUNCTION BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



DETAILED DESCRIPTION

The AAT1614 consists of a Boost converter, an internal LDO, four channel current sink controller with balancing, and PPM (PWM to PWM) dimming control logic for applications in LCD panel backlight.

Shutdown Control (EN)

The AAT1614 can be disabled to reduce the supply current to 10µA when EN pin is pulled low, and can be powered up when EN pin is at high level. Note that when the EN pin is left floating, the AAT1614 is still disabled via an internal pull-low resistor.

Under Voltage Lockout (UVLO)

For systematic startup, AAT1614 employs a UVLO threshold of 2.35V. Thus, the input supply must exceed the UVLO threshold for the regulators to begin startup. Likewise, the device shuts down all functions when the input voltage is lower than UVLO falling threshold of 2.2V. A 150mV hysteresis is added to prevent device chattering when the input supply is noisy or unstable during power up or power down.

Boost Regulator for VLED

The boost regulator uses a peak current mode control scheme that provides fast output response during transients, and also simple compensation. With an integrated low R_{DSON} (typical 0.2Ω) NMOS, build-in soft start, and adjustable switching frequency from 500kHz to 2MHz, this boost regulator is a compact and economical solution but also provides design in flexibility. The boost regulator operates from a minimum input voltage of 3V, and delivers an output voltage that reaches the maximum capable duty cycle. The duty cycle (D) is calculated by

$$D = \frac{V_O - V_I}{V_O} \quad \text{or} \quad \frac{V_O}{V_I} = \frac{1}{1-D}, \quad (V_O = \text{VLED})$$

Where V_O (VLED) is the output of the boost regulator. Typical maximum duty cycle is approximately 92%.

At the heart of the current mode topology are two feedback loops. See the AAT1614 Boost Regulator Functional Block Diagram Figure 1.

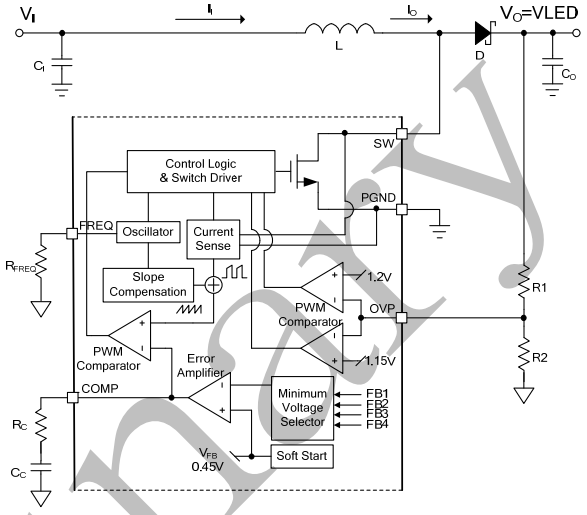


Figure 1. Boost Functional Block Diagram

One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal power switch. The second loop monitors the voltage via minimum voltage selector between LED current sink controller FB1 to FB4 and compares the minimum voltage to an internal reference voltage of 0.45V using a transconductance error amp. Regulation is achieved by modulating the internal power switch ON time. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles above 50%. During each rising edge of the internal clock pulse, the power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

Boost Current Limit

When the Boost NMOS switch current exceeds 2.5A, the current limit function disables the gate driver of this boost regulator and prevents the internal NMOS from switching. Once switch current falls below the 2.5A threshold, the boost will resume switching. The current limit value is clamped to a lower value at power-on and will reach the final value of 2.5A after soft-start.

Internal Soft Start

AAT1614 employs a soft-start feature to limit the inrush current. The build-in soft-start circuit prevents the excessive inrush current, input voltage drop and output voltage overshoot. The typical soft-start time is 5ms~9ms.

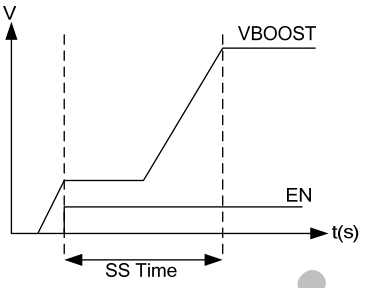


Figure 2. Soft-Start Timing Chart

Boost Switching Frequency

The switching frequency of AAT1614 can be set from 500kHz to 2MHz by an external resistor connected from the FREQ pin to GND. The switching frequency (f_{OSC}) vs. the resistor value (R_{FREQ}), is shown below.

Table 1

Boost Frequency (kHz)	R_{FREQ} (kΩ)
2,000	22
1,750	26
1,500	32
1,250	40
1,000	51
750	75
500	120

Compensation Selection (R_C & C_C)

To stabilize the boost regulator's loop, a RC series network is added from the COMP output pin to analog ground. See Figure 1. R_C is chosen to set the amplifier gain for a targeted crossover frequency. Setting the total loop gain to unity gain at the desire crossover frequency, we can calculate R_C by approximately

$$R_C = 0.3 \times \frac{V_O}{V_{FB}} \times \frac{V_O}{V_I} \times \frac{\pi \times f_C \times C_O}{g_m \times g_{CS}}$$

Where g_m=105μS is the feedback error amplifier transconductance, g_{CS}=4S is the current sense transconductance, the crossover frequency of the regulator f_C=20%×f_{RHPZ}, and V_{FB} is the feedback reference voltage of 0.45V. In typical application, R_C value ranges from 500Ω to 20kΩ.

Once R_C is selected, C_C is adjusted to place a zero for neutralizing the output pole caused by the output capacitance C_O and load R_O. Use the following equation to calculate C_C,

$$C_C = \frac{C_O \times R_O}{50 \times R_C}$$

In typical application, C_C value ranges from 22nF to 68nF.

Over Voltage Protection

The AAT1614 offers a programmable over-voltage protection to prevent over-voltage damage to the IC and other components. The over-voltage protection voltage (VLED_OVP) is set via external resistor ladder from Boost output VLED to ground with the center tap connected to OVP pin to compare to an internal reference of 1.2V. When the voltage exceeds 1.2V, the Boost will stop switching until the voltage falls below the OVP threshold. As shown in Figure 1, the over-voltage protection voltage VLED_OVP is determined using the following formula:

$$VLED\_OVP = V_{OVP} \times \left(1 + \frac{R1}{R2}\right) \text{ where } V_{OVP} = 1.2V$$

The variation of LED forward voltage is an important factor to consider when calculating the required OVP. For example, to drive N pieces of LEDs per channel, with a LED forward voltage V_{FD}, consider the worst case LED forward voltage variation by adding a margin of error. To determine the external OVP resister R1 (upside) and R2 (downside), an example formula is as followed:

$$\frac{R_1}{R_2} = \frac{V_{FD} \times (N+2) + V_{FB}}{V_{OVP}} - 1 = K, \ (V_{FB} = 0.45V)$$

LED Current Sink Controller

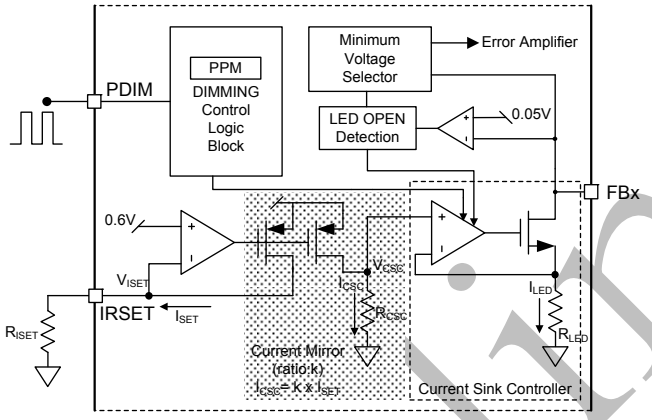


Figure 3. Current Sink Control Functional Block Diagram

LED Current Programming

The LED current set point is chosen by connecting an external resistor from the IRSET pin to ground. The voltage at the IRSET pin is set to 0.6V and the channel current is calculated according to this equation:

$I_{SET} = \frac{V_{ISET}}{R_{ISET}}$ and $I_{CSC} = k \times I_{SET}$ where k is the internal current mirror ratio. Please refer to Figure 3.

$V_{CSC} = I_{CSC} \times R_{CSC} = I_{LED} \times R_{LED}$, since the voltages are the same at the non-inverting and the inverting inputs of the current sink controller op amp.

Solving for I_{LED} and substituting for I_{CSC},

$$I_{LED} = \frac{I_{CSC} \times R_{CSC}}{R_{LED}} = \frac{k \times V_{ISET} \times R_{CSC}}{R_{LED}} \times \frac{1}{R_{ISET}}$$

$$I_{LED} = \frac{95}{R_{ISET}} \text{ where } \frac{k \times V_{ISET} \times R_{CSC}}{R_{LED}} = 95$$

R_{ISET} is in kΩ and I_{LED} is the current of each channel in mA .

The channel current (I_{LED}) vs. the resistor value (R_{ISET}), is shown below.

Table 2. I_{LED} V.S. R_{ISET}

LED Current (mA)	R_{ISET} (kΩ)
40	2.375
30	3.17
25	3.8
20	4.75
10	9.5

PWM to PWM Dimming (PPM)

The AAT1614 offers PPM (PWM to PWM) dimming for controlling the LED brightness via external PWM dimming signal. The algorithm of PPM is that LED current is synchronized with PDIM input logic signal and there is no phase delay between each current sources. See Figure 4 for reference.

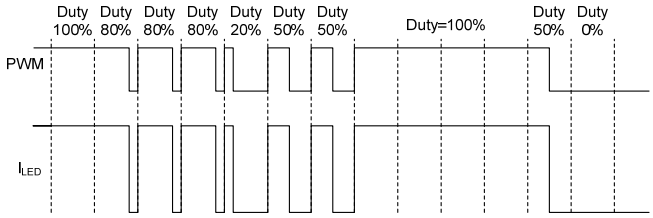


Figure 4. PPM Dimming Timing Chart

LED Brightness Control

The AAT1614 also features pulsed dimming control with PWM frequency from 120Hz to 30kHz. For the PWM frequency range from 120Hz to 1kHz, the minimum dimming duty is about 1%. For the PWM frequency range from 1kHz to 10kHz, the minimum dimming duty is about 5%, For the PWM frequency near 30kHz, the minimum dimming duty is about 10%. The range of PWM dimming duty is shown below.

Table 3. Dimming Frequency V.S. Duty Cycle

f_{PDIM} (Hz)	D_{MIN}	D_{MAX}
120<f≦1k	1%	100%
1k<f≦10k	5%	100%
10k<f<30k	10%	100%

LED Open-Circuit Protection

When one or more LED strings are open, the FBx voltage of the open channel will be pulled low and the COMP pin will be driven high. The boost converter duty cycle and the output voltage will increase. Once the boost output voltage rises high enough to reach the OVP threshold, and simultaneously the FBx voltage keeps below the LED Open Detection Voltage of 0.05V, the open LED channels will be turned off, and will be turned on again after FBx voltage higher than 0.05V..

Thermal Shutdown (OTP)

When the temperature reaches 150°C, AAT1614 will quickly discharge the soft-start capacitor, turn off the power NMOS and the current regulators. The shutdown condition can be removed after the temperature falls below 110°C and the power is cycled.

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1614.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VIN pin. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VIN bypass capacitor should refer to analog ground (AGND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost regulator contains the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node SW. The input bulk capacitance should also be placed close to these power path components to shorten the power ground length between the input and output.

Feedback and Compensation Components

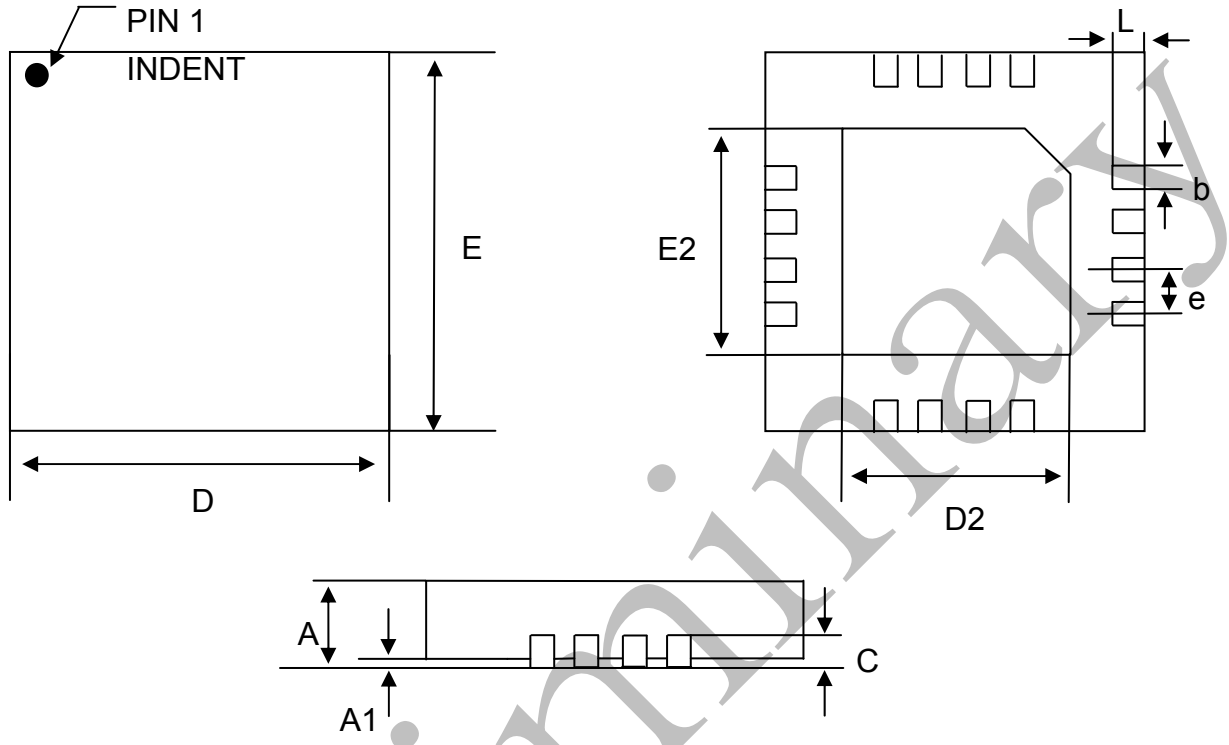
Any components for feedback, such as the resistive divider networks for setting the output voltage, should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise pickup. Likewise, compensation components should be placed as close as possible to the pin or device.

Ground Plane

Use a power ground plane for the boost output capacitor ground, for the boost input bulk capacitor ground, and PGND pin. All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create an analog ground plane for VIN pin, bypass capacitor grounds, compensation component ground, feedback resistive network grounds, and also the AGND pin. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (AGND) and power ground (PGND) should be connected only at one signal point, near the expose pad by shorting the AGND pins to the expose pad.

PACKAGE DIMENSION

WQFN16L-3x3



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	-	0.20	-
D	2.90	3.00	3.10
D2	1.65	1.70	1.75
E	2.90	3.00	3.10
E2	1.65	1.70	1.75
e	-	0.50	-
L	0.35	0.40	0.45